R836
High Performance
DTV Silicon Tuner
Datasheet

Rafael Micro

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Rafael Micro
R836 High Performance DTV Silicon Tuner

General Description

In heritage from Rafael Micro's state-of-the-art architecture, the R836 DTV silicon tuner, no need for external RF balun, can achieve best linearity with lowest power consumption. R836 offers unmatchable RF performance for all digital broadcast television standards including DVB-T/T2/C, J.83B, ATSC, DTMB and ISDB-T/C. With innovative AccuTune™ and TrueRF™ mechanisms, R836 provides superior performance in sensitivity, linearity, adjacent channel immunity, and image rejection. The chip embeds a smart tracking filter and power detector to optimize different input channels and power scenarios as well as the spurious free dynamic range.

The R836 is a highly integrated silicon tuner that builds in low noise amplifier (LNA), mixer, fractional PLL, VGA, voltage regulator and tracking filter, eliminating the need for external SAW filters, LNA and RF Balun. High performance LNA, and small package enable R836 the perfect solution for both cost and performance sensitive applications.

With proprietary GreenRF techniques, R836 achieves both high performance and the lowest power consumption which perfectly compliant with the worldwide trend. The R836 comes in a small and thin QFN RoHs compliant package.

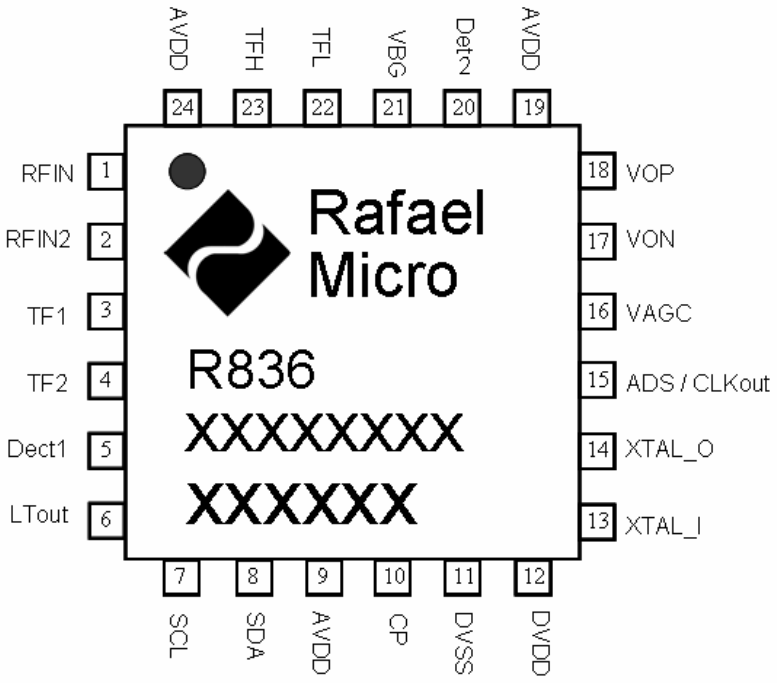
Features

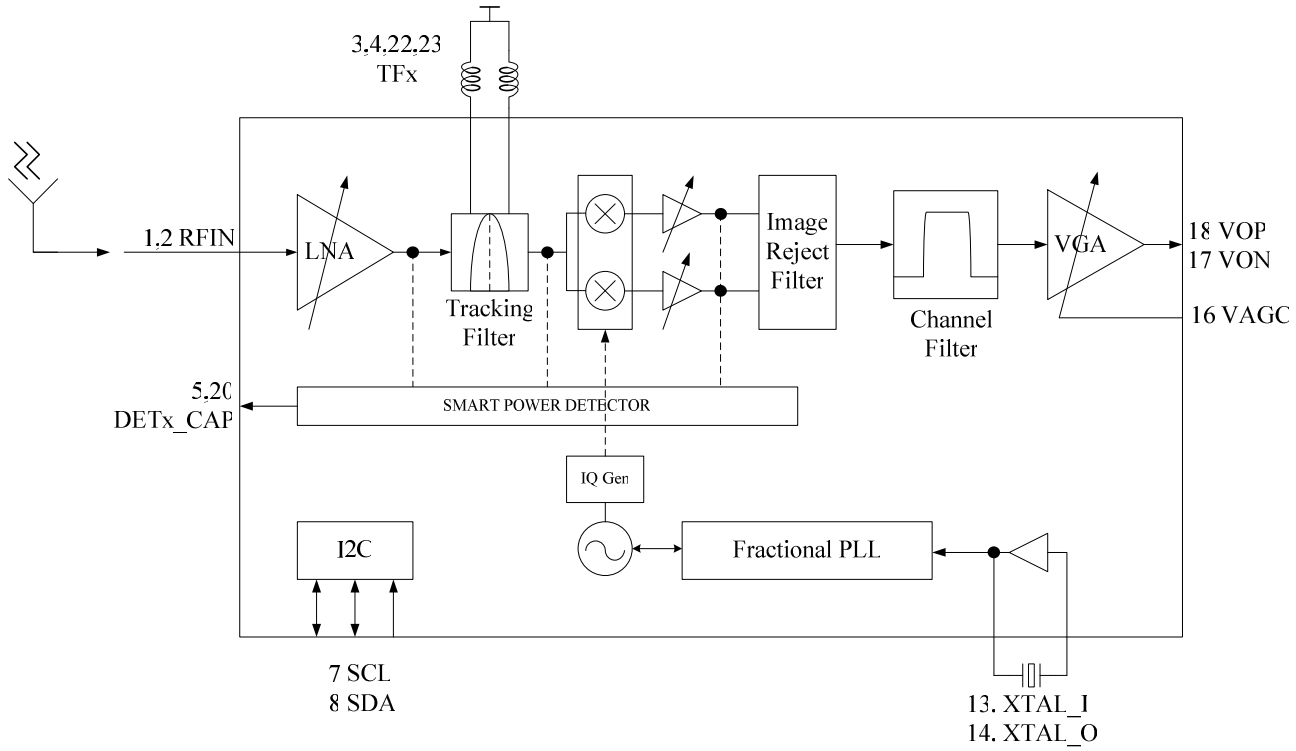
- Worldwide digital TV tuner
  - DVB-T/T2/C, ISDB-T/C, DTMB, ATSC,J.83B
- Compliant with worldwide specifications
  - NorDig, D-BOOK, C-BOOK, ARIB, EN55020, OpenCable™
- All system channel support
  - 42MHz to 1002MHz
- Lowest BOM cost
  - No required SAW, external LNA and RF balun
- Low power consumption
  - 200mA when supply by Vcc=3.3V
- Crystal oscillator output buffer for single crystal application
- Best-in-class adjacent channel immunity in real-world to overcome all rigorous field environments.
- Standard I^2C control interface

Applications

- Terrestrial DTV (DVB-T/T2, DTMB, ISDB-T, ATSC)
- Cable DTV (DVB-C, J83B, ISDB-C).

Functional Block Diagram





The architecture of the tuner is illustrated in the block diagram showed above. To achieve world-class far-away-interference rejection performance, R836 use unique single-end LNA design to achieve low NF & high linearity at the same time. The following tracking filter stage auto-tunes the center frequency to optimize the input quality of the wanted channel. With Rafael Micro's smart power detector and >65dB image rejection filter, R836 can operate on highly interference environment and easily pass digital standards at the same time. The real world rejection ability can exceed MOPLL-based CAN-tuner.

Figure A: Example of DTV Reception for PCTV Applications

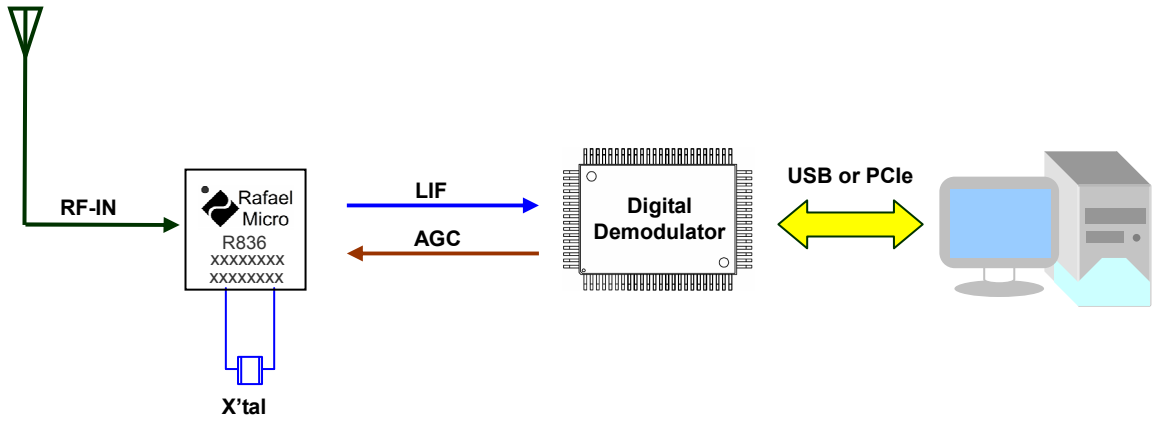
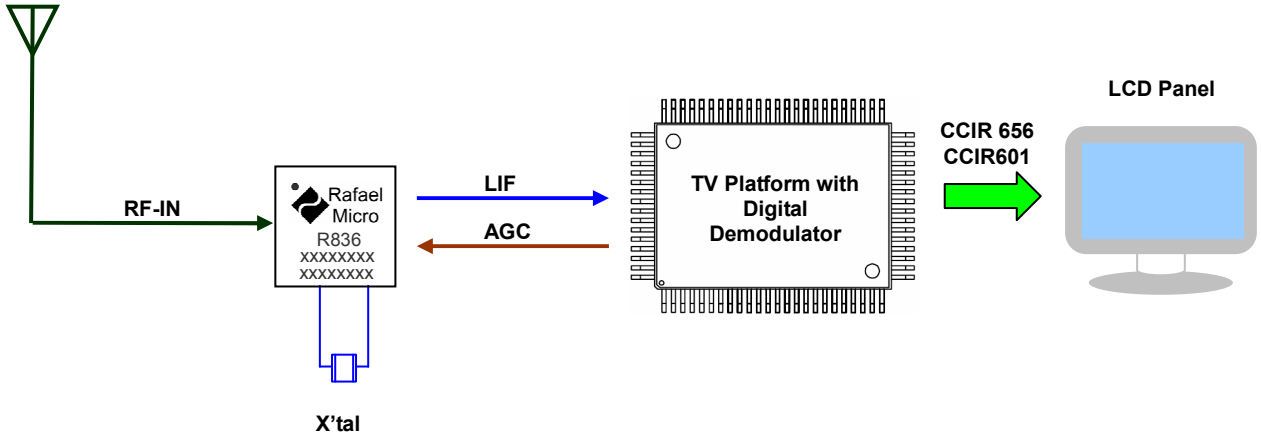


Figure B: Example of DTV Reception for LCD TV Applications



Contents

1 Specifications

1.1 Recommend Operation Condition

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3	3.3	3.6	V
Address Select	AS	0		3.3	V
AGC Control	V_{AGC}	0		3.3	V

1.2 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	-0.3	3.6	V
I^2C input voltage	Vi2c	-0.3	3.6	V
Operation Temperature	T_{OP}	0	85	℃
Storage Temperature	T_{STG}	-65	150	℃

1.3 DC Characteristics

Characteristic	Symbol	Min	Typ	Max	Units
Total Current Consumption[1]	I_{CC}		200	220	mA
Stand-by current (LT on)[12]	I_{SB}		33	40	mA
Power-down current[1]	I_{PD}		10		mA
I/O High Level Input Voltage	V_{IH}	1.7		3.6	V
I/O Low Level Input Voltage	V_{IL}	0		1.3	V
I/O High Level Output Voltage	V_{OH}	2.7		3.6	V
I/O Low Level Output Voltage	V_{OL}	0		0.2	V

1. These data are measured under Vcc=3.3V

2. stand-by current is measured under Loop through function is turned ON

1.4 ESD Immunity Abilities

Characteristic	Symbol	Min	Max	Units
ESD Protection (Charge Device Model)	CDM	200		V
ESD Protection (Human Body Model)(1)	HBM	2K		V
Latch-Up Immunity	LU	300		V

1.5 Tuner AC Characteristics

Parameters	Symbol	Condition	Units	Min	Typical	Max
System						
Input Return Loss	S11	All Gain	dB		-8	
Operation Frequency Range	f_{in}		MHz	42		1002
Frequency Tuning Step	F_{step}	16MHz Crystal	Hz		488.3	
Channel Bandwidth	BW		MHz		6,7,8	
Noise Figure	NF		dB		2.9	
Gain Control Range	AGC		dB		109	112
In-Band $IIP3$[1]	$IIP3_{IB}$	N±1 N±2	dBm	-14	-7	
Out-of-Band $IIP3$[1]	$IIP3_{OOB}$	N±6 N±12	dBm	0	+8	
Image Rejection	IR		dBc		65	
Composite Triple Beat[2]	CTB	110 Channel at 75dBuV	dBc		-65	
Composite Second Order[2]	CSO		dBc		-65	
Multiple Crystal Frequency Spurious	X_{spur}	Refer to RF-In	dBm		-130	
Adjacent Channel Rejection	ACI N+-1	DVB-T,64QAM,CR3/4	dBc		-46	
	DCI N+-1	DVB-T,64QAM,CR:3/4	dBc		-42	
IF Output Level	IF_{OUT}	Swing	Vp-p	0.7	1	1.5
		Impedence		Differential 2kΩ//5pF		
Loop-Through						
RF Frequency Range	f_{LT}		MHz	42		1002
LT Gain	G_{LT}		dB	1	2.2	3
Synthesizer						
PLL Locking time	T_{PLL}		ms			5
Phase Noise @ 860MHz (DTV mode)	PN_{LO}	1K	dBc		-89	
		10K	dBc		-98	
		100K	dBc		-110	
Clock-output Swing	CLKout	Oscilloscope loading 11pF	mV		450	

1. Performed with RFAGC frozen at maximum LNA gain and minimum IF gain using 6MHz channel spacing. These values are measured at worst case frequencies.

2 Pin Description

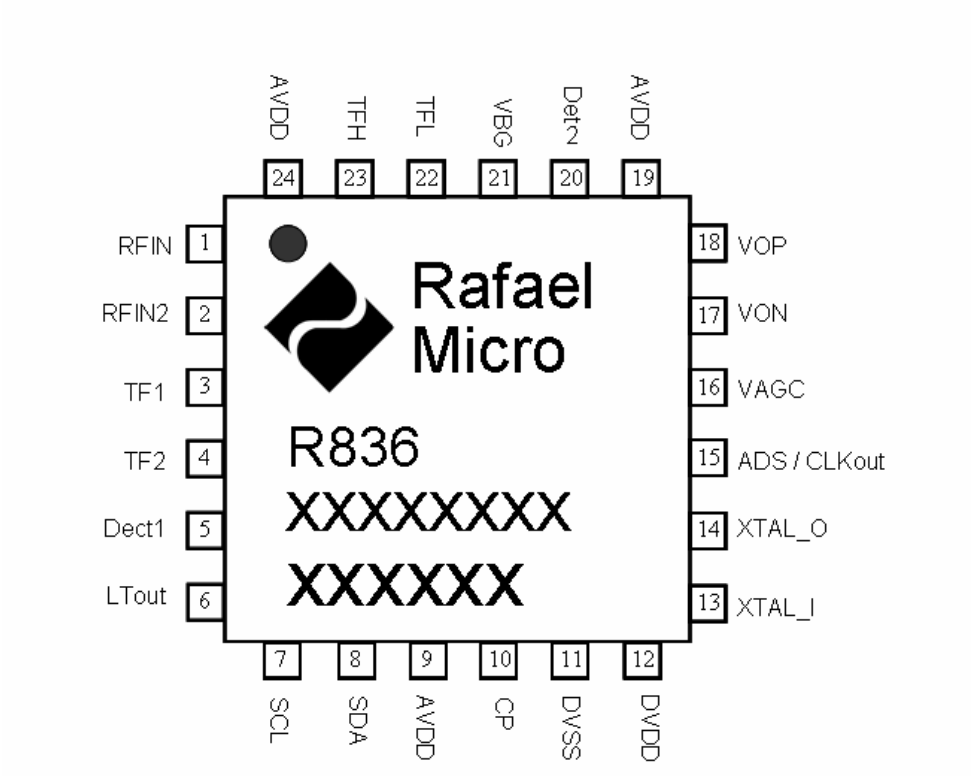


Figure 2-1 : Pin Allocation of R836 Silicon Tuner

Table 2-1 : R836 Summary List of Pin Assignment

Pin Number	Symbol	I/O	Description
1,2	**RFIN, RFIN2**	I	RF input
5,20	**Detx**	-	Power detector decoupling capacitor
3,4,22,23	**TFxx**	-	Tracking filter pin out
6	**LTout**	O	Loop Through output
7	**SCL**	I	I2C bus, clock input
8	**SDA**	I/O	I2C bus, data input/ output
9	**AVDD**	S	AVDD for PLL
10	**CP**	-	PLL Charge Pump decouple
11	**DVSS**	S	Digital Ground
12	**DVDD**	S	Digital 3.3V Supply
13	**XTAL_I**	I	Crystal Driver Input
14	**XTAL_O**	I	Crystal Driver Output
15	**ADS / CLKout**	I/O	Address pin or Clock buffer output
16	**VAGC**	I	IF automatic gain control input
17,18	**VOP, VON**	O	Differential IF output
19	**AVDD**	S	Analog 3.3V supply
21	**VBG**	-	Internal 1.2V decouple
24	**AVDD**	S	RF 3.3V Supply

(note: E-Pad is GND)

3 Programming and Registers

3.1 I2C Series Programming Interface

The programmable features of the R836 are accessible through an I^2C compatible serial interface. Bi-directional data transfers are programmed through the serial clock (SCL) and serial data lines (SDA) at a standard clock rate of 100 KHz and up to 400KHz.

Data Transfer Logic

The I^2C control byte includes a fixed 7-bit slave address ID and a read/write (R/W) bit. Fixed slave address ID is 0x34 or 0x74, according to Pin15 connection. R836 I2C address is 0x34 while Pin15 connecting to GND; address is 0x74 while Pin15 floating. The R/W bit is set 0 for write and 1 for read. Write mode and read mode will be further explained in the following sections.

I^2C Write/Read Address

Table 3-1 : I^2C Write Address

Mode	I^2C Address(Bin)							R/W	Address (Hex)
	MSB							LSB	
Write	0	0/1	1	1	0	1	0	0	0x34 or 0x74
Read	0	0/1	1	1	0	1	0	1	0x35 or 0x75

Write Mode

When the slave address matches the I^2C device ID with write control bit , I^2C start interprets the following first byte as first written register address. These following bytes are all the register data (page write I^2C control). Register 0, 1 and 2 are reserved for internal use only and can be written by I^2C write command.

Figure 3-1 : The Typical Write Mode Sequence

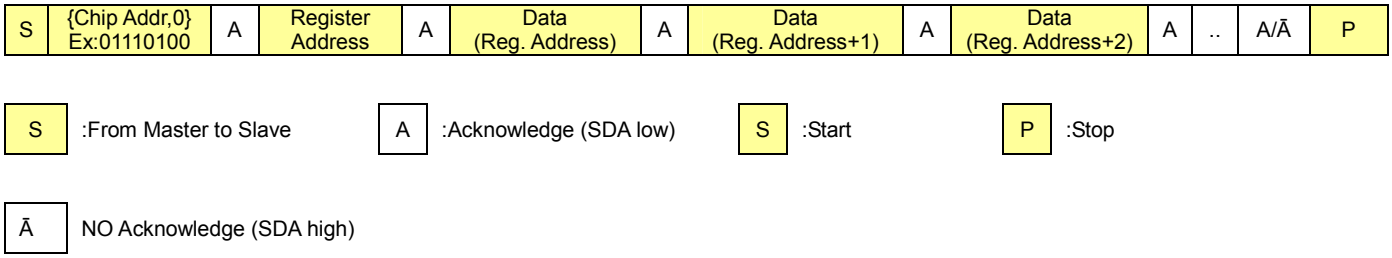
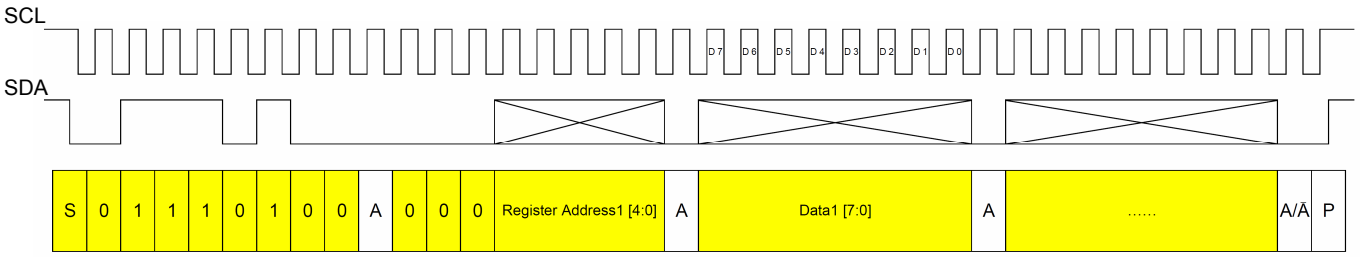


Figure 3-2 : An Example of Write Mode Procedure



Read Mode

When the slave address matches the I^2C device ID with read control bit, data are immediately transferred after ack command. Reading data transmission begins from core register 0 to final register until “P”(Stop) occurs. The data is transmitted from LSB to MSB, and the data of register 0, which is 0x96, is fixed as reference check point for read mode.

Figure 3-3 : The Typical Read Mode Sequence

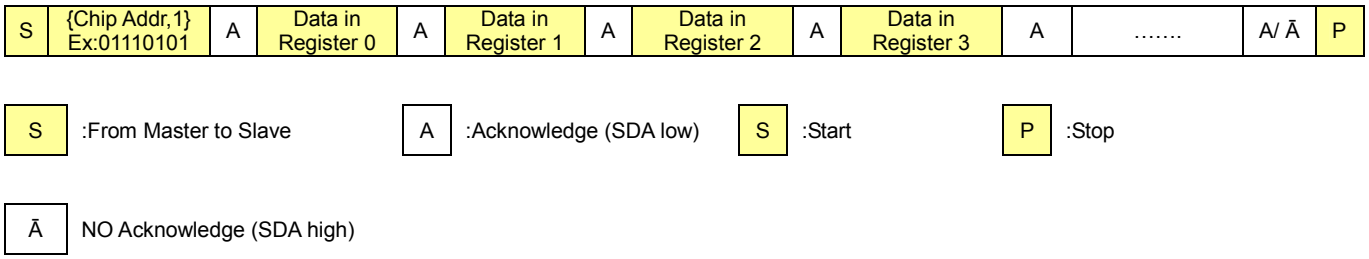
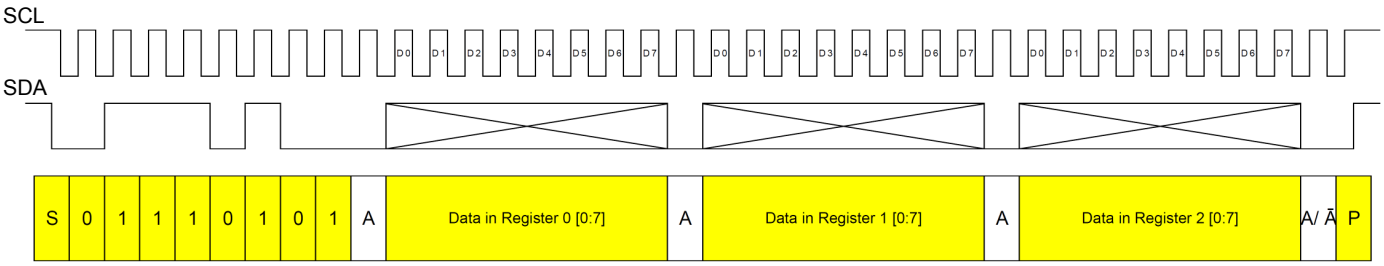


Figure 3-4 : An Example of Read Mode Procedure



4 Application Information

4.1 Application Circuit

Please contact Rafael Micro System Integration Engineering for the detailed application circuit and BOM list. For different system applications, Rafael Micro provides customized engineering services for the reference design, RF layout, Gerber file and even the PCB review. These engineering services are recognized as a great value to shorten time to market cycle.

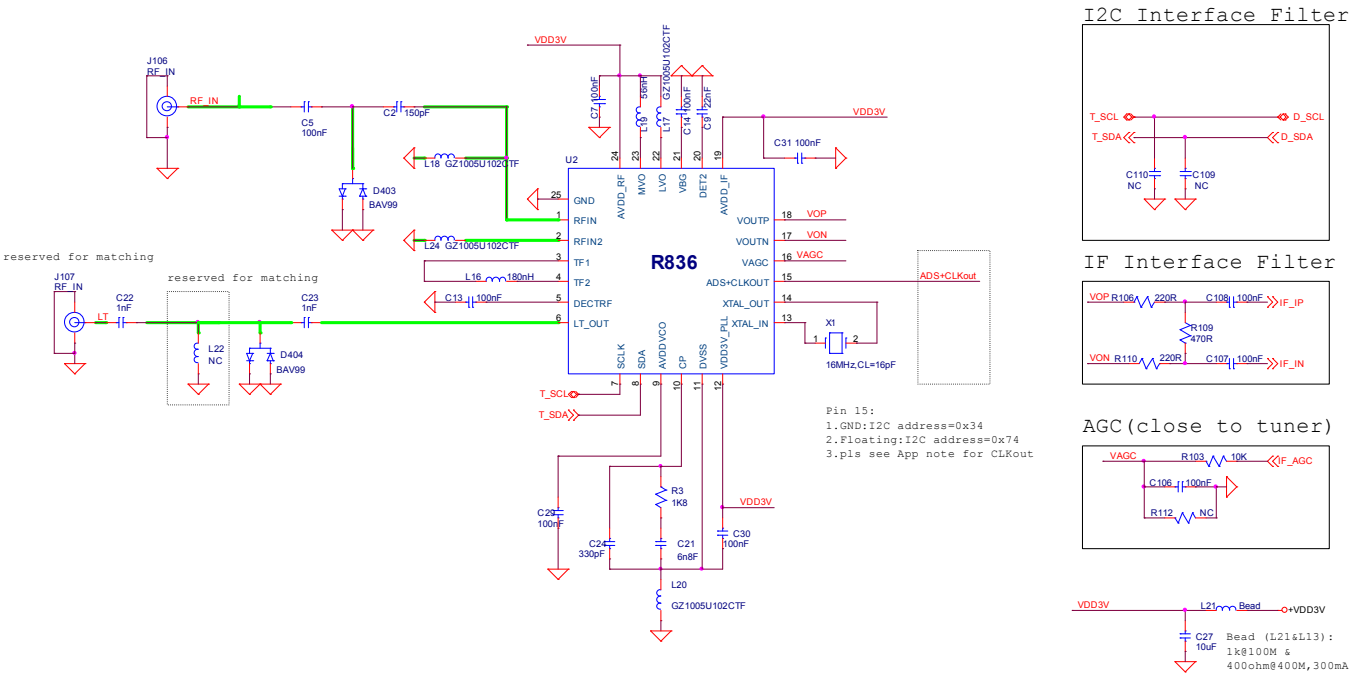


Figure 4-1 : R836 reference schematic

4.2 IF Frequency

R836 down-converts the RF signal to a low-IF frequency. The low-IF frequencies for different standards are shown in Table 4-1.

Table 4-1: IF Frequency Table

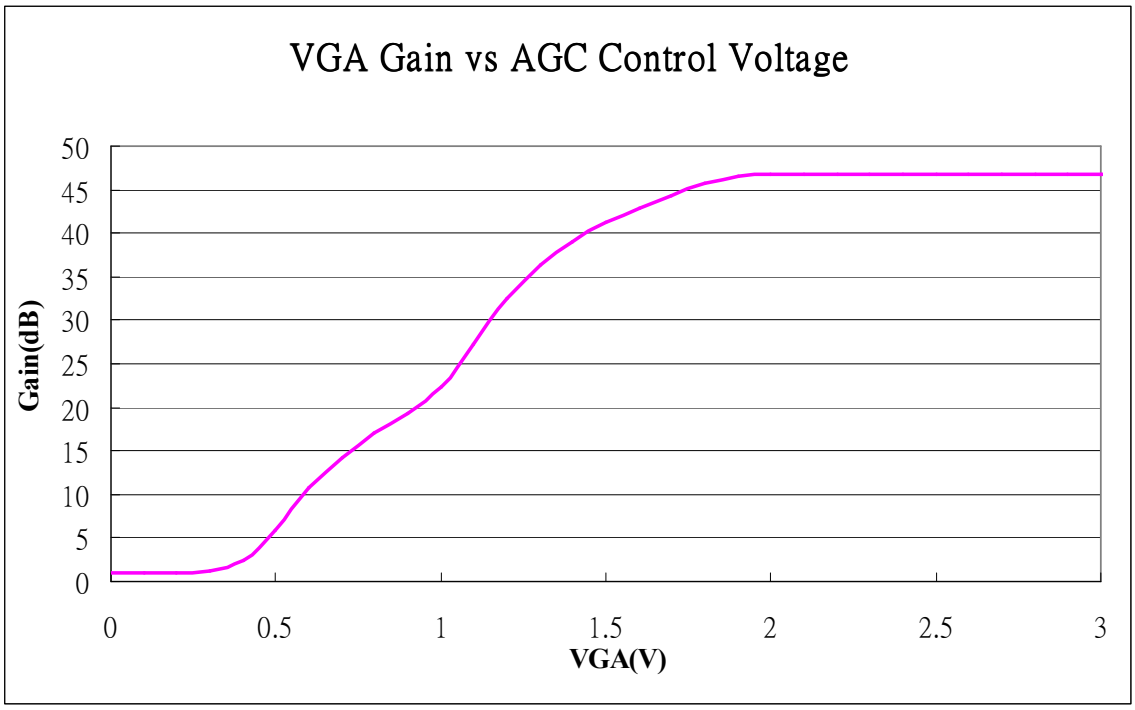
	TV Standard	Channel BW	Video / Center
1	ATSC	BW = 6MHz	Fcenter= 5.07 MHz
2	DVB-T/T2 6M	BW = 6MHz	Fcenter= 4.57 MHz
3	DVB-T/T2 7M	BW = 7MHz	Fcenter= 4.57 MHz
4	DVB-T/T2 8M	BW = 8MHz	Fcenter= 4.57 MHz
5	DVB-C 6M	BW = 6MHz	Fcenter= 5.07 MHz
6	DVB-C 8M	BW = 8MHz	Fcenter= 5.07 MHz
7	ISDB-T	BW = 6MHz	Fcenter= 4.063 MHz
8	DTMB	BW = 8MHz	Fcenter= 4.57 MHz
9	DVB-T2 1.7M	BW = 1.7MHz	Fcenter= 1.90 MHz
10	DVB-T2 10M	BW = 10MHz	Fcenter= 5.60 MHz

4.3 AGC Control

The R836 has built-in RFAGC to achieve the optimal SNR while minimizing distortion. When RF input power increases, the internal power detector is activated to attenuate internal LNA gain to an optimal level. On the other hand, when RF input power decreases, internal power detector will increase internal LNA gain to achieve good picture quality.

The IF amplifier and IFAGC pin are available for controlling by demodulators. R836 provides a wide range of IF amplifier gain from +1dB to +47dB. And the corresponding IFAGC voltage range is from 0.3V to 2V. The relationship between IF amplifier gain and input voltage is shown in figure 4-2.

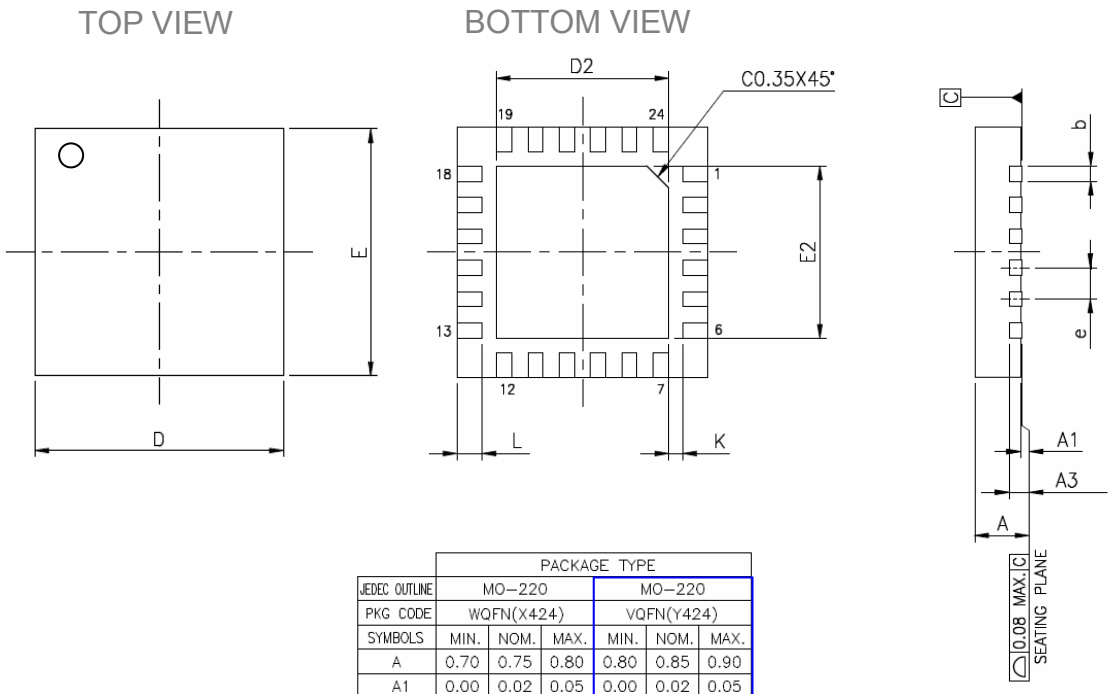
Figure 4-2 : VGA Gain vs AGC control Voltage



5 Package Dimensions and Outline

The R836 is packaged by a Lead-Free 4x4 24-pin Quad Flat No-Lead (QFN) package. The detail package dimensions are listed in Figure 5-1.

Figure 5-1 : R836 Package Dimensions and Outline



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X424)			VQFN(Y424)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.18	0.25	0.30	0.18	0.25	0.30
D	4.00 BSC			4.00 BSC		
E	4.00 BSC			4.00 BSC		
e	0.50 BSC			0.50 BSC		
K	0.20	—	—	0.20	—	—

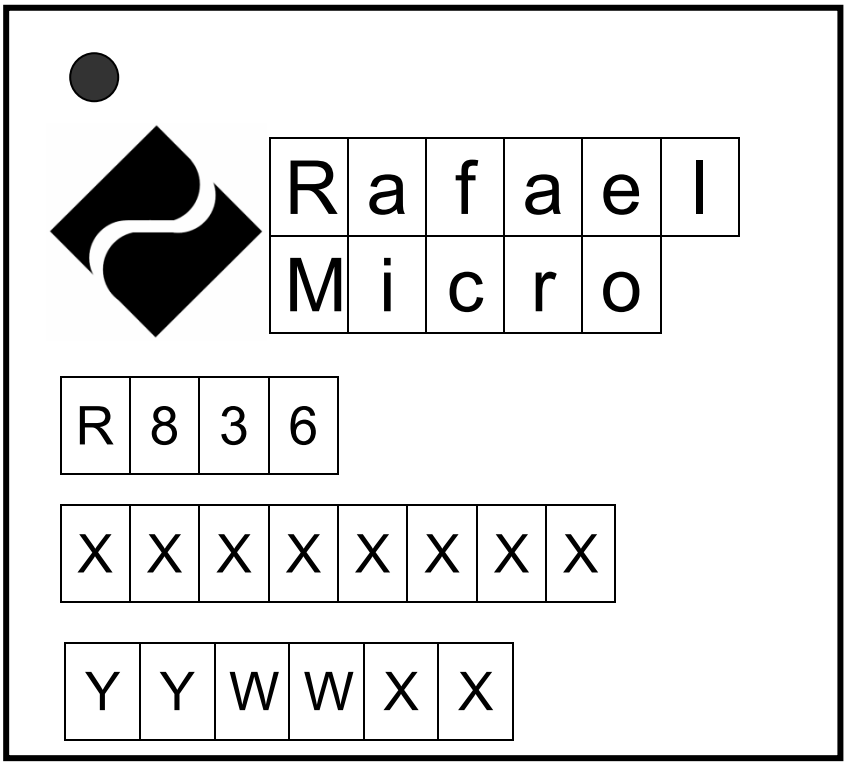
	E2			D2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
112X112 MIL	2.15	2.25	2.30	2.15	2.25	2.30	0.35	0.40	0.45	V	X	W(V)GGD-8
113X113 MIL	2.50	2.60	2.65	2.50	2.60	2.65	0.35	0.40	0.45	X	V	W(V)GGD-6
114X114 MIL	2.60	2.70	2.75	2.60	2.70	2.75	0.35	0.40	0.45	V	X	W(V)GGD-6
8 115X115 MIL	2.40	2.50	2.55	2.40	2.50	2.55	0.35	0.40	0.45	V	X	W(V)GGD-8
120X120 MIL	2.50	2.60	2.65	2.50	2.60	2.65	0.275	0.325	0.375	V	X	W(V)GGD-8

Note:

Before soldering to system board, R836 need to be baked at 125°C for more than 8 hours to eliminate moisture contamination.

6 Top Marking

6.1 R836 Top Marking



6.2 Top Marking Explanation

Mark Method	Laser	
Font Size:	Logo：3.1X1.3mm Device Number：0.45X0.3mm Mfg Code& Date Code：0.45X0.3mm	
Line 1 Marking	Circle=0.3 mm Diameter (Top-left justified)	Pin 1 identifier
Line 2 Marking	Rafael Micro Logo	Rafael Micro
Line 3 Marking	Device Number	R836
Line 4 Marking	(1) XXXXXXXX = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. By Assembly have different Manufacturing code
Line 5 Marking	YYWWXX YY = Year ; WW = Work Week XX= Control Code	Assigned by the Assembly House. Corresponds to the year and work week of the mold date. Rafael Micro internal control code.

7 Crystal Requirements

The crystal frequency for R836 is 16 MHz. The R836 is well accompanied with traditional DIP package crystal. To reduce component count and font factor, a low profile SMD package crystal is recommended.

Table 7-1 : Crystal Specifications

Parameter	Min	Typical	Max	Units
Frequency Range	-	16	-	MHz
ESR			50	Ω
Frequency accuracy		± 30	± 50	ppm
Load Capacitor (CL)	-	16	-	pF
Input level to XTAL_P pin when using external clock	120		3300	mVp-p

Ordering Information

Part Number	Description	Package Type
R836	High Performance Digital TV Silicon Tuner	QFN4x4-24

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Revision History

Revision	Description	Owner	Date
1.0	First release	Cliff Huang	2013/06/11
1.1	Add TOP Marking in chap 6	Jason Wang	2013/06/18