MxL201RF

Digital Cable Tuner Reference Design

Version 5.2

August 27, 2010

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1. Introduction and Block Level Diagram

This document introduces the reference design of the MxL201RF silicon tuner. The MxL201RF is able to convert 44-1002 MHz RF input signal to IF frequencies ranging from 4 to 44 MHz. The tuner allows programmable channel bandwidths of 6, 7, or 8 MHz. The IC also supports various crystal frequencies ranging from 16MHz to 50MHz. By default 48MHz crystal is used to provide the optimal phase noise performance. The MxL201RF can be used for standard digital cable applications (ITU-T J.83 Annexes A [DVB-C] and C and B [US Cable], DOCSIS, and EURODOCSIS) as well as standard digital terrestrial applications (DVB-T/H, ATSC, and DMB-T/H).

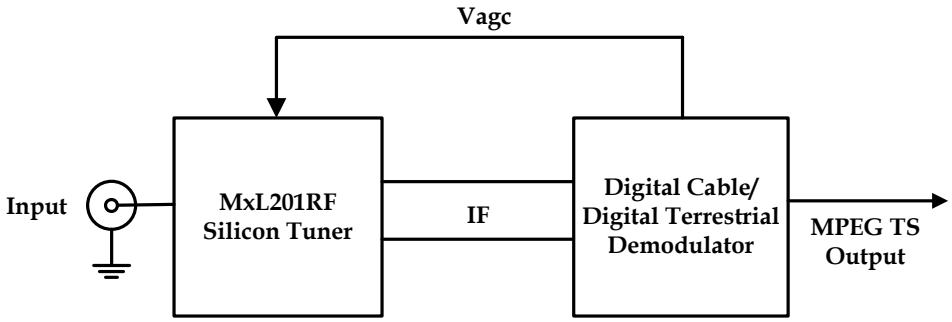

Figure 1 – MxL201RF in single-tuner digital cable/terrestrial applications

Figure 1 shows MxL201RF operating in standard single-tuner digital cable/terrestrial applications. The tuner can be configured to either low-IF or high-IF output (low-IF is preferred for the optimal performance) with single AGC control.

2. Recommended Power Supply Options

The MxL201RF tuner can operate with either a single voltage supply (3.0-3.6V) in standard mode as shown in Figure 2, or dual voltage supplies (3.0-3.6V and 1.7-2.0V) in low-power mode, as shown in Figure 3. The MxL201RF uses two on-chip linear regulators to provide 1.6 V supply and one on-chip linear regulator to provide the 1.2 V supply.

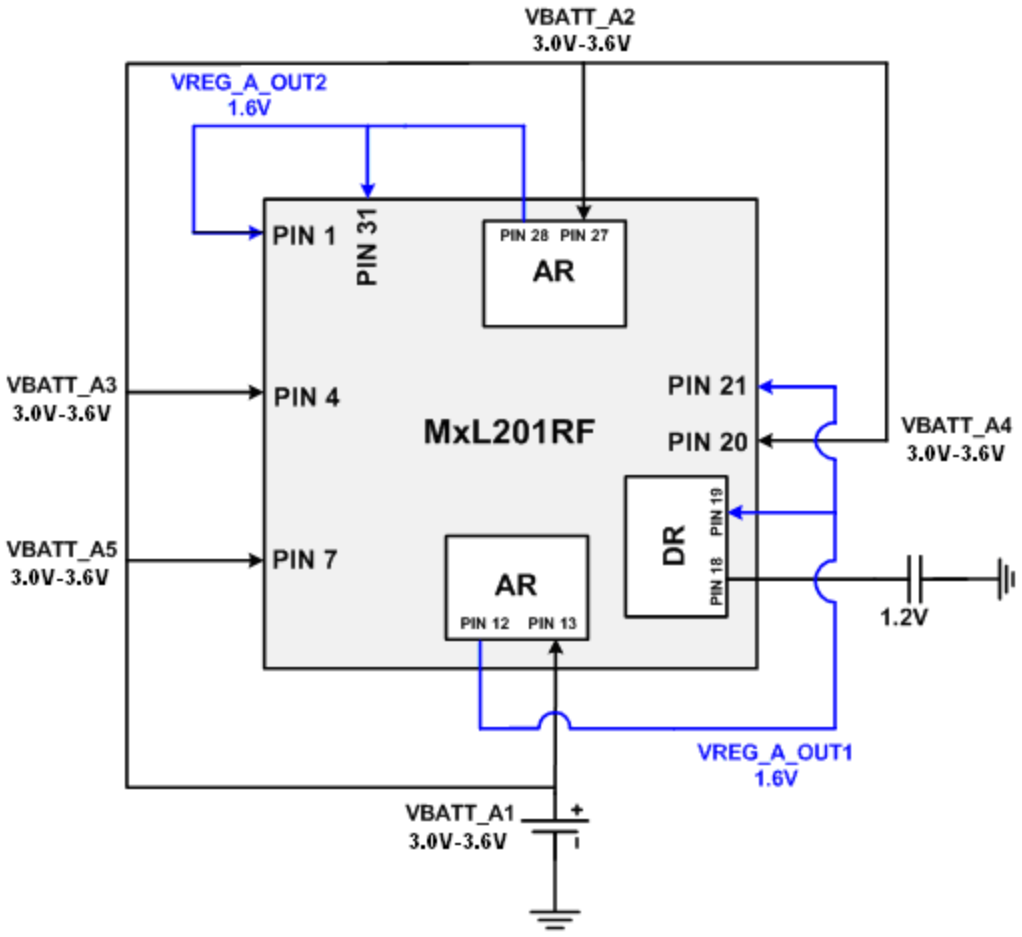

Figure 2 – Power supply configuration diagram of standard-power mode

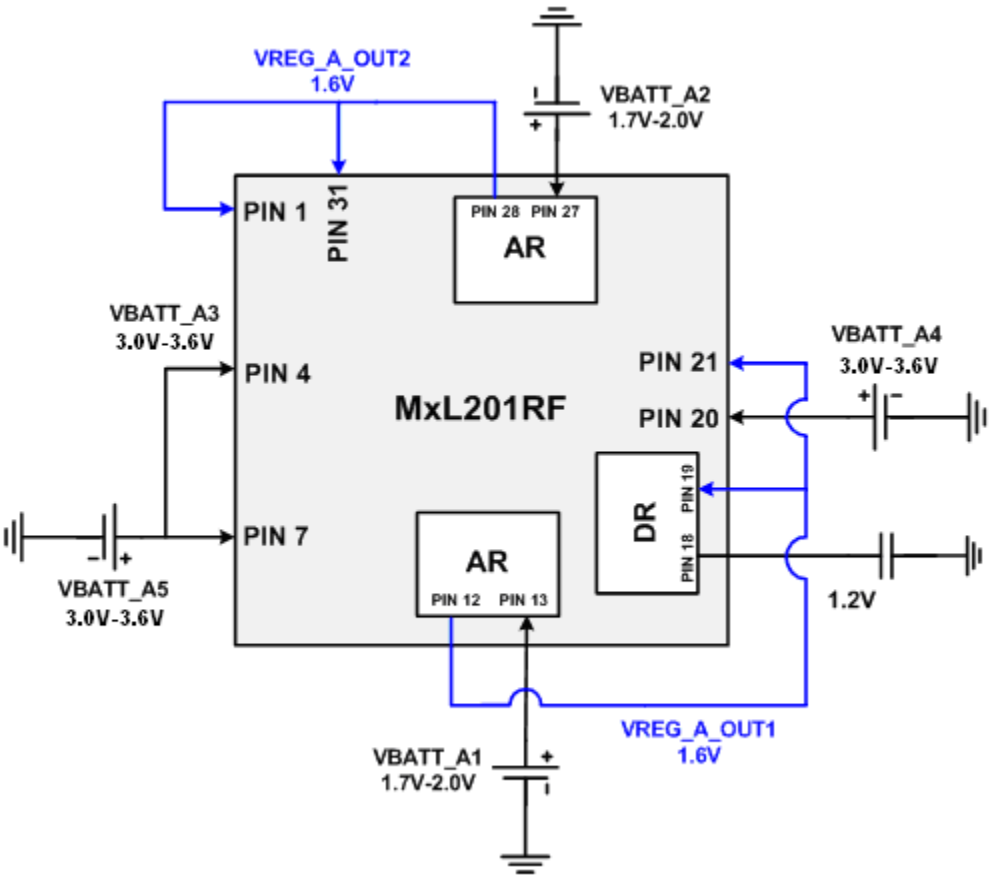

Figure 3 – Power supply configuration diagram of low-power mode

Table 1 below shows the power consumption estimate for the two different supply configurations. The power consumption of MxL201RF can be minimized by providing 1.7-2.0V (1.8V nominal) to VBATT_A1, A2 and 3.0-3.6V (3.3V nominal) to VBATT_A3, A4, and A5. Please note the power consumption estimate shown in Table 1 is based on the following assumptions:

1) MxL201RF tuner is operating in digital cable mode at UHF frequency
2) VBATT_A1, A2 = 3.3V for standard-power configuration.
   VBATT_A1, A2 =1.8V for low-power configuration.
   VBATT_A3, A4, A5 = 3.3V for both standard-power and low-power configuration.

Table 1 – Power consumption estimate of MxL201RF

	VBATT_A1 + A2 (Estimate)	**VBATT _A3 +A4 + A5 (Estimate)**	**Total Power Consumption (Estimate)**
Standard-Power Configuration	3.0V – 3.6V 150 mA	3.0V – 3.6V 43 mA	3.3V * 193mA (637 mW)
Low-Power Configuration	1.7V – 2.0V 150 mA	3.0V – 3.6V 43 mA	1.8V * 150mA + 3.3V * 43mA (412 mW)

3. Reference schematics

Figure 4 shows the reference schematic of MxL201RF.

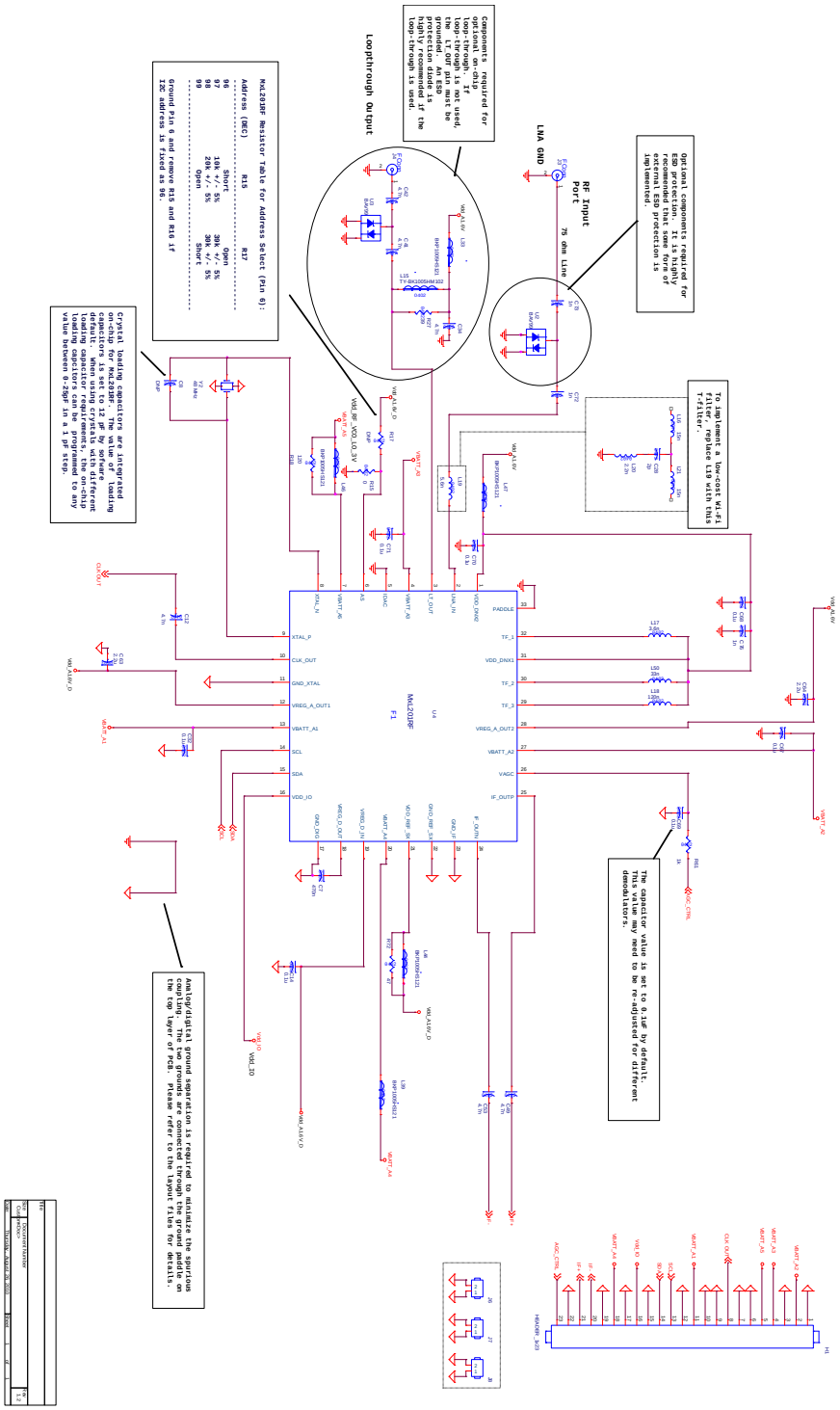

Figure 4 – Reference schematic of MxL201RF

1) **RC filter on Vagc line**

   The capacitor (C69) of the RC filter on the Vagc line is 0.1uF by default. The capacitor value may need to be optimized for different demodulators.

2) **Analog/Digital ground separation**

   In order to minimize the on-board spur coupling from digital circuits to analog circuits, a separate digital/analog grounding strategy in PCB layout shall be applied. Please refer to physical layout example for details and strictly follow the physical layout example to avoid performance degradation.

3) **Integrated on-chip crystal loading capacitors**

   For MxL201RF the crystal loading capacitors have been integrated on-chip as shown in Figure 5, to minimize the level of crystal harmonic related spurs. The value of loading capacitors ranges from 1-25pF in 1 pF steps and is programmable via I²C. In the case where a loading capacitance greater than 25 pF is required, an external capacitor may be placed in parallel with the crystal and designated by the C8 placeholder in the schematic. Upon power-up of the IC, the loading capacitors are set to the hardware default of 10pF. At this time, there will be a small crystal frequency offset if 10pF is not the desired loading capacitance value. The offset can be resolved after programming the capacitors to the desired value via the I²C. The current MxL201RF evaluation control software default sets the capacitors to 12pF, the optimal value for Mercury X32-48.000 crystal used in MxL-144 evaluation board. Optimization may be required when different crystals are used in the design.

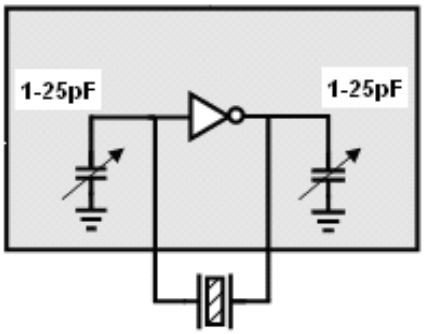

Figure 5 – Integrated on-chip crystal loading capacitors

4) **ESD Protection Diodes**

Included in the reference schematic is an ESD protection diode for the RF input. This ESD diode is highly recommended to prevent ESD damage to the tuner. A recommended ESD diode (BAV99) for use is listed in the Bill of Materials.

5) **On-Chip Loop Through**

There is the option of using the on-chip loop-through of the MxL201RF shown in the schematic. The additional components required are listed in the Bill of Materials in Table 2. If the on-chip loop-through is not to be used, then pin 3 (the loop-through output) of the tuner must be grounded. An ESD protection diode should also be added on the loop-through path, to protect the chip from ESD damage.

6) **Wi-Fi Filter (Optional)**

If a Wi-Fi filter is needed, a low-cost filter can be implemented by replacing L19 with a T-filter. See reference schematic for details. The additional components required are listed in the Bill of Materials in Table 2.

4. Bill of Materials (BOM)

Table 2 lists the BOM of MxL201RF. This BOM corresponds to the reference schematic in Figure 4 and separates the additional components required to make use of the loop-through. Components with the DNP (do not populate) designation in the schematic are not listed in the BOM.

Table 2 – BOM list of the reference schematic

Item	Qty	Reference	Part Description	Manufacturer Part Number
1	1	C7	470nF Capacitor (0402)	GRM155R61A474KE15D (Murata)
2	3	C12,C49,C53	4.7nF Capacitor (0402)	GRM155R71E472KA01D (Murata)
3	7	C14,C32,C67,C68, C69,C70,C71	0.1uF Capacitor (0402)	GRM155R71C104KA88D (Murata)
4	2	C63,C64	2.2uF Capacitor (0603)	ECJ-1VB1A225K (Panasonic)
5	3	C72, C73, C76	1nF Capacitor (0402)	GRM155R71E102KA01D (Murata)
6	1	J3	F Connector	
7	1	L17	3.6nH Inductor (0402)	HK10053N6S-T (Taiyo Yuden)
8	1	L18	120nH Inductor (0402)	HK1005R12J-T (Taiyo Yuden)
9	1	L19	5.6nH Inductor (0402)	HK10055N6J-T (Taiyo Yuden)
10	4	L39, L44,L46, L47	Ferrite Bead	BKP1005HS121 (Taiyo Yuden)
11	1	L50	33nH Inductor (0402)	HK100533NJ-T (Taiyo Yuden)
12	1	R15	0 Ohm Resistor (0402)	RC-402JR-070RL (Yageo)
13	1	R18	120 Ohm Resistor (0402)	RC-402JR-07470RL (Yageo)
14	1	R61	1k Ohm Resistor (0402)	RC-402JR-071KL (Yageo)
15	1	R72	47 Ohm Resistor (0402)	RC-402JR-0747RF (Yageo)
16	1	U2	ESD Protection Diode	BAV99 T/R (NXP)
17	1	U4	RF Tuner IC	MaxLinear MxL201RF 32-pin
18	1	Y2	48 MHz Crystal (SMD)	Mercury X32-48.000
Components Required for Loop-Thru (Optional)				
19	3	C34, C41, C42	4.7nF Capacitor (0402)	GRM155R71E472KA01D (Murata)
20	1	J4	F Connector	
21	1	L15	Ferrite Bead (0402)	BK1005HM102 (Taiyo Yuden)
22	1	L33	Ferrite Bead (0402)	BKP1005HS121 (Taiyo Yuden)
23	1	R27	39 Ohm Resistor (0402)	RC402JR-0739RL(Yageo)
24	1	U3	ESD Protection Diode	BAV99 T/R (NXP)
Components Required for Wi-Fi Filter (Optional)				
25	2	L16, L21 (+/- 5% Tolerance)	15nH Inductor (0402)	LQG15HS15NJ02D (Murata)
26	1	L20 (+/- 5% Tolerance)	2.2nH Inductor (0402)	LQG15HS2N2S02D (Murata)
27	1	C28 (+/- 0.1pF Tolerance)	2.0pF Capacitor (0402)	UMK105CG020BW (Taiyo Yuden)

The reference design excluding loop through requires 32 components, including the MxL201RF tuner IC, as shown in Table 2. An additional 7 components (excluding the F- connector) are required to properly make use of the on-chip loop-through. To avoid performance degradation, the recommended tolerances of the following components have to be met.

1) L17, L18, L50, L16, L21, and L20: ± 5% for optimal filtering performance
2) C28: ± 0.1pF for optimal filtering performance
3) R15 and R17: ± 5% if I²C addresses 97 or 98 are used
4) Crystal Y2: ± 30ppm for optimal performance
5) Supply pin ferrite beads – BKP1005HS121 or equivalent component
   Loopthrough ferrite beads – BK1005HM102 or equivalent component.
   See ferrite bead specifications listed in Table 3.

Table 3 – Specification of ferrite beads

FB Type/Spec	Max. DC Resistance	Min. AC Impedance (50-1000MHz)
Ferrite beads for supply pins (L33, L39, L44, L46, L47)	0.2 Ω	100 Ω
Ferrite bead for on loop-through (L15)	1.0 Ω	250 Ω

5. PCB layout guidelines

It is strongly recommended copying the reference layout for any design using 201RF. In the cases where it is difficult to completely copy the reference layout, the following PCB layout rules shall be obeyed in order not to introduce performance degradation from noise and spur coupling. Any deviations from the reference layout will need to be reviewed by the local MaxLinear FAE.

Analog/Digital ground separation

In order to minimize the spur coupling from digital circuits to analog circuits, which results in performance degradation, the digital ground/analog ground separation is required to be implemented in the PCB layout. The analog and digital grounds are connected only through the ground paddle on the top layer, as depicted in Figure 6 and Figure 7. In Figure 6, the MxL201RF's 5 ground pins are connected through the paddle ground. Figure 7 shows the total separation of the digital ground and analog ground. For a NIM design, the analog ground of the tuner should remain isolated while the digital ground of the tuner and the ground of the demodulator are shared.

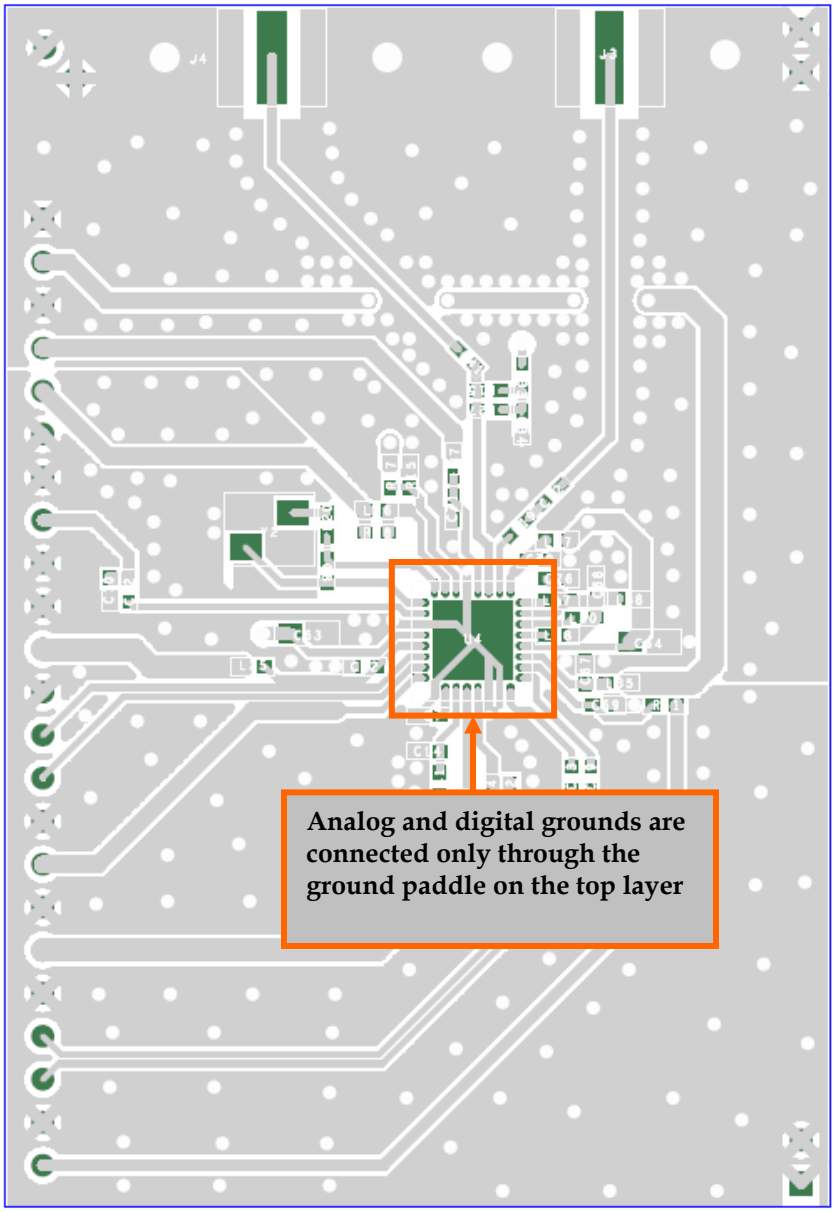

Figure 6 – Top layer view of analog/digital ground connection

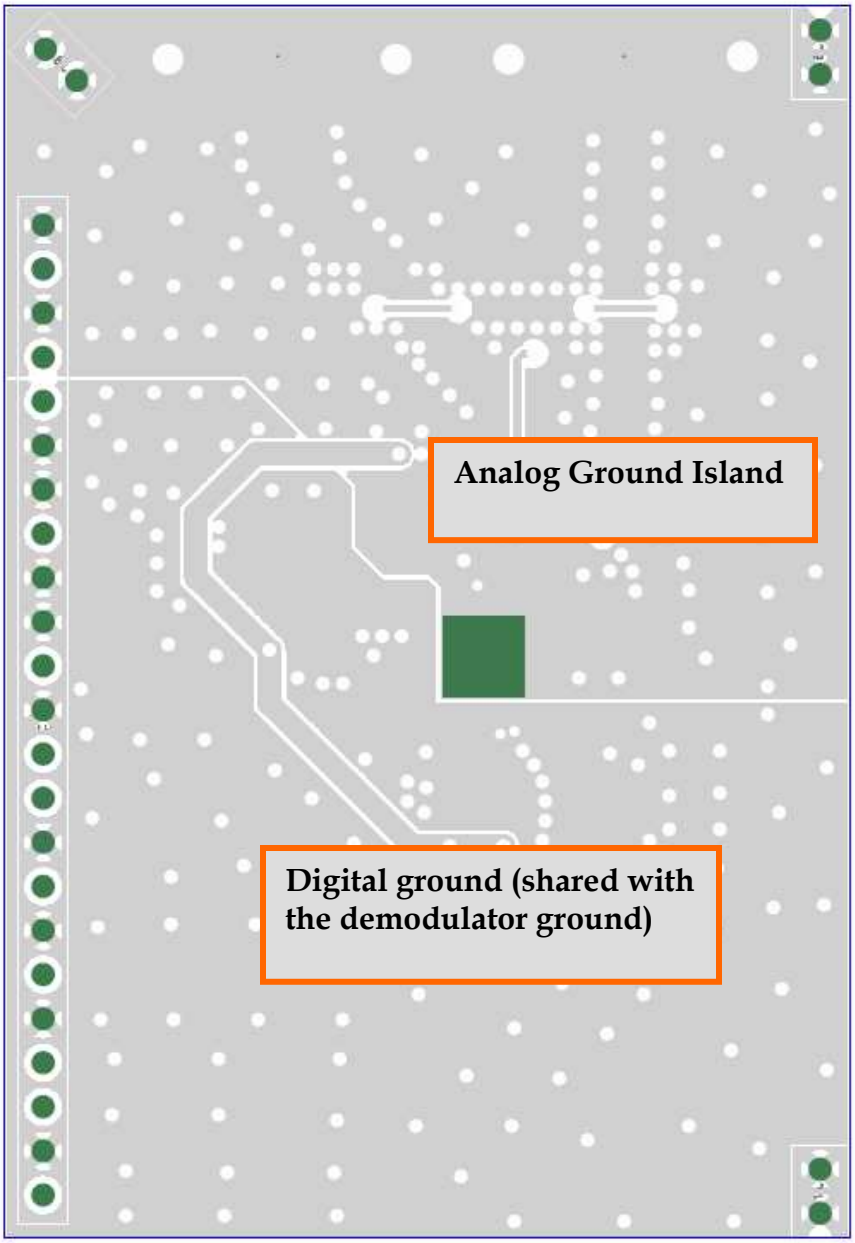

Figure 7 – Bottom layer view of analog/digital ground separation

RF Input Trace:

- The characteristic impedance Z_0 of the RF input trace needs to be designed to be 75Ω in order for the optimal input impedance match. It is also recommended using co-planar waveguide instead of micro-strip transmission line for the RF input trace for better noise isolation. Various free CAD tools are available for calculating the characteristic impedance for PCBs with different stack-ups.
- Multiple ground stitching vias are required around the RF input trace in order to minimize the potential spur coupling. Ground vias are shown as white dots in Figure 8 below.

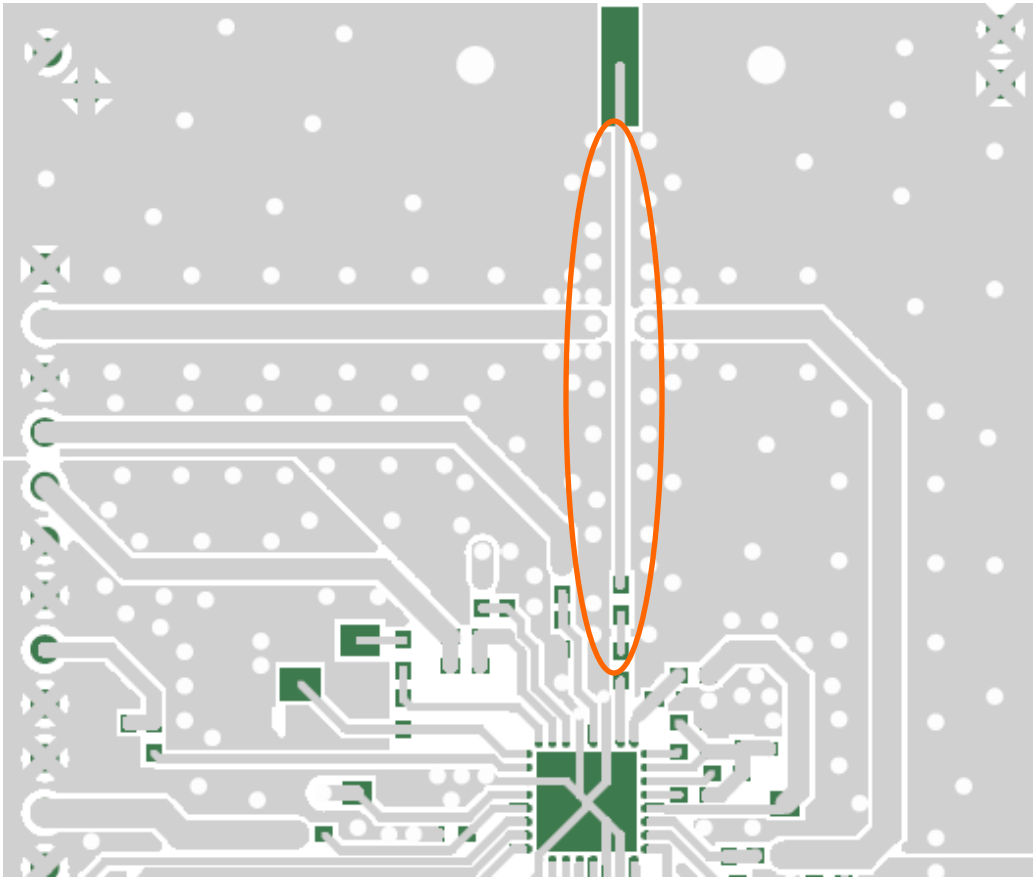

Figure 8 –Multiple ground vias around the RF input trace

- The RF input trace should be kept straight-lined. If right-angle turns are needed for the RF input trace routing, 45° right-angle bends should be used in order to minimize the junction mismatch of the transmission line. A zigzag pattern shall be avoided.

Differential IF output traces

- The differential IF output traces shall be routed in symmetry to minimize the imbalances between IF+/IF- and placed close to each other in order for canceling out the radiation.

Component Placement

- Tracking filter inductors (L17, L18, and L50) need to stay as close as possible to the IC in order to minimize the noise coupling. The component orientation shall exactly follow the reference layout, as shown in Figure 9.
- Bypass capacitor (C7) of VREG_D_OUT shall stay as close as possible to the IC and be placed in perpendicular to the RF input trace, as shown in Figure 9.
- All ferrite beads and other bypass capacitors should stay as close as possible to the IC in order to minimize the noise/spur coupling.
- The external RC filter (C69 and R61) for AGC line should be placed close to the IC, as shown in Figure 9.

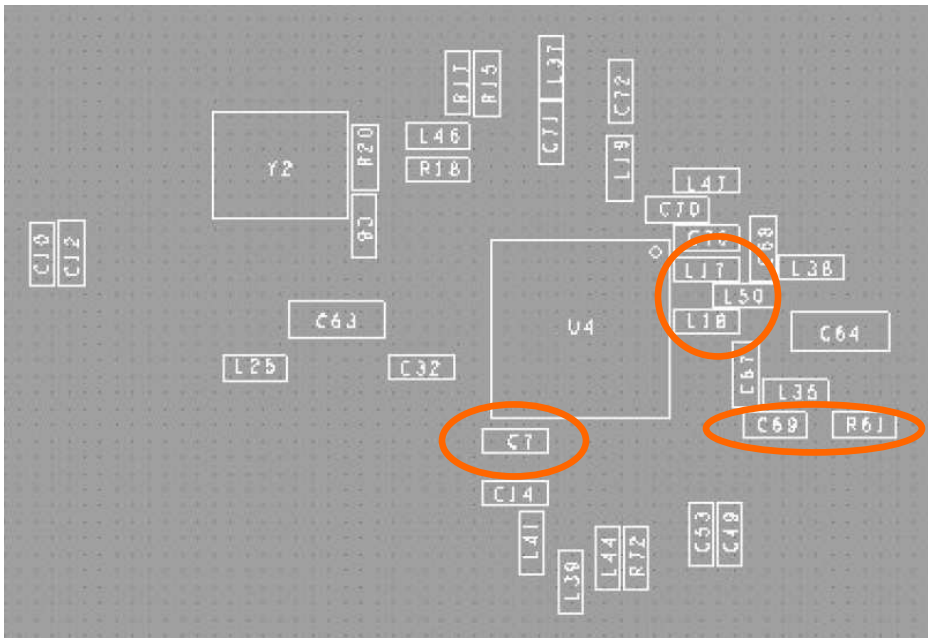

Figure 9 – PCB Layout component placement recommendation

6. Physical Layout Example

The layout examples of MxL201RF show the component placement for the MxL201RF implementation with loop-through (MxL149 Reference Design Board). In addition, 2 and 4-layer layout examples, without loop-through circuitry, are provided (MxL144 Reference Board Design). Routing and trace information can be found in the Gerber file list described in section 6. The use of 4-layer PCB is recommended for optimal performance. Please refer to the appropriate Gerber file for layout details. Figure 10 and Figure 11 show the top/bottom layer component placement of the reference schematic in Figure 4.

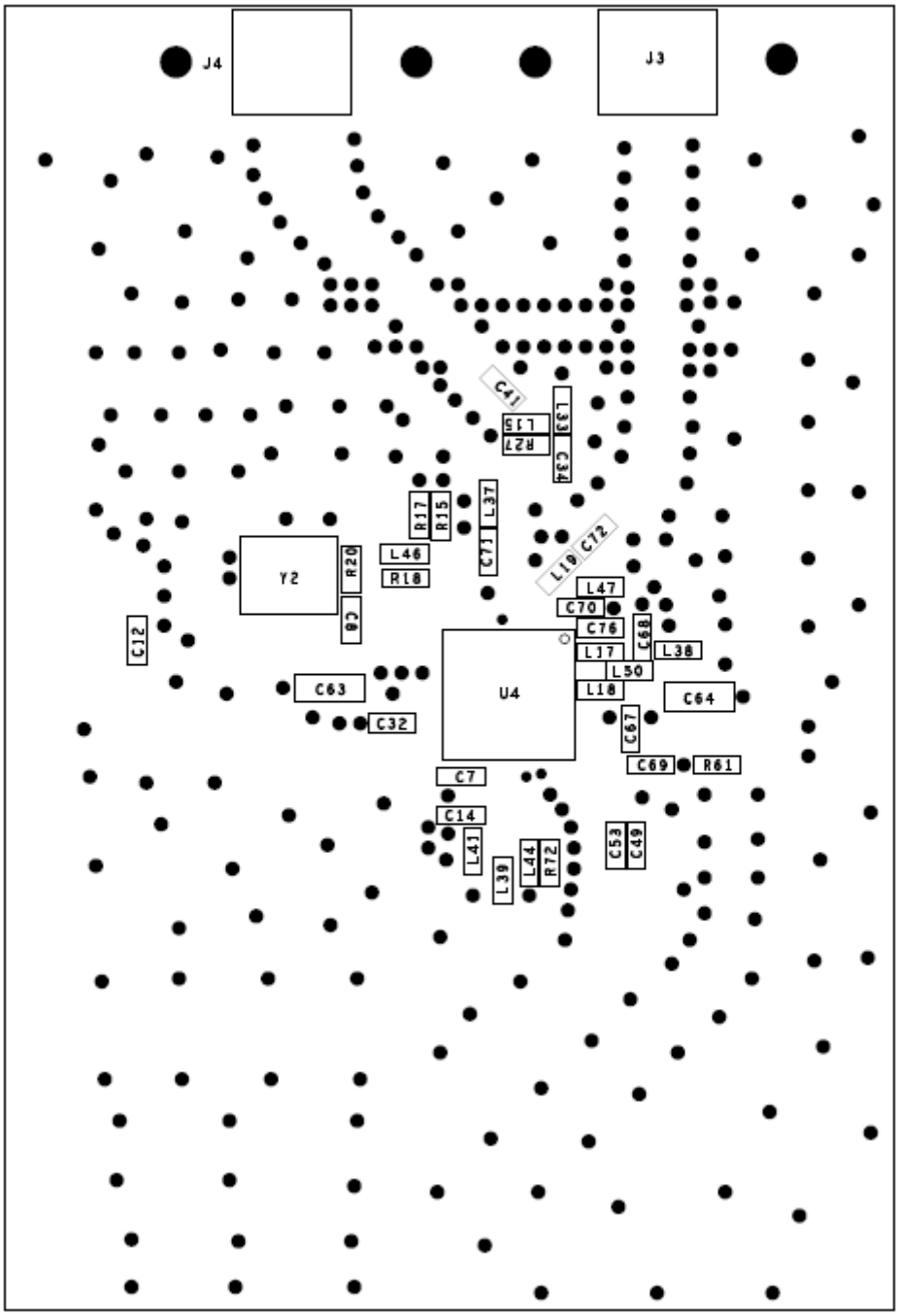

Figure 10 – MxL201RF component placement top layer

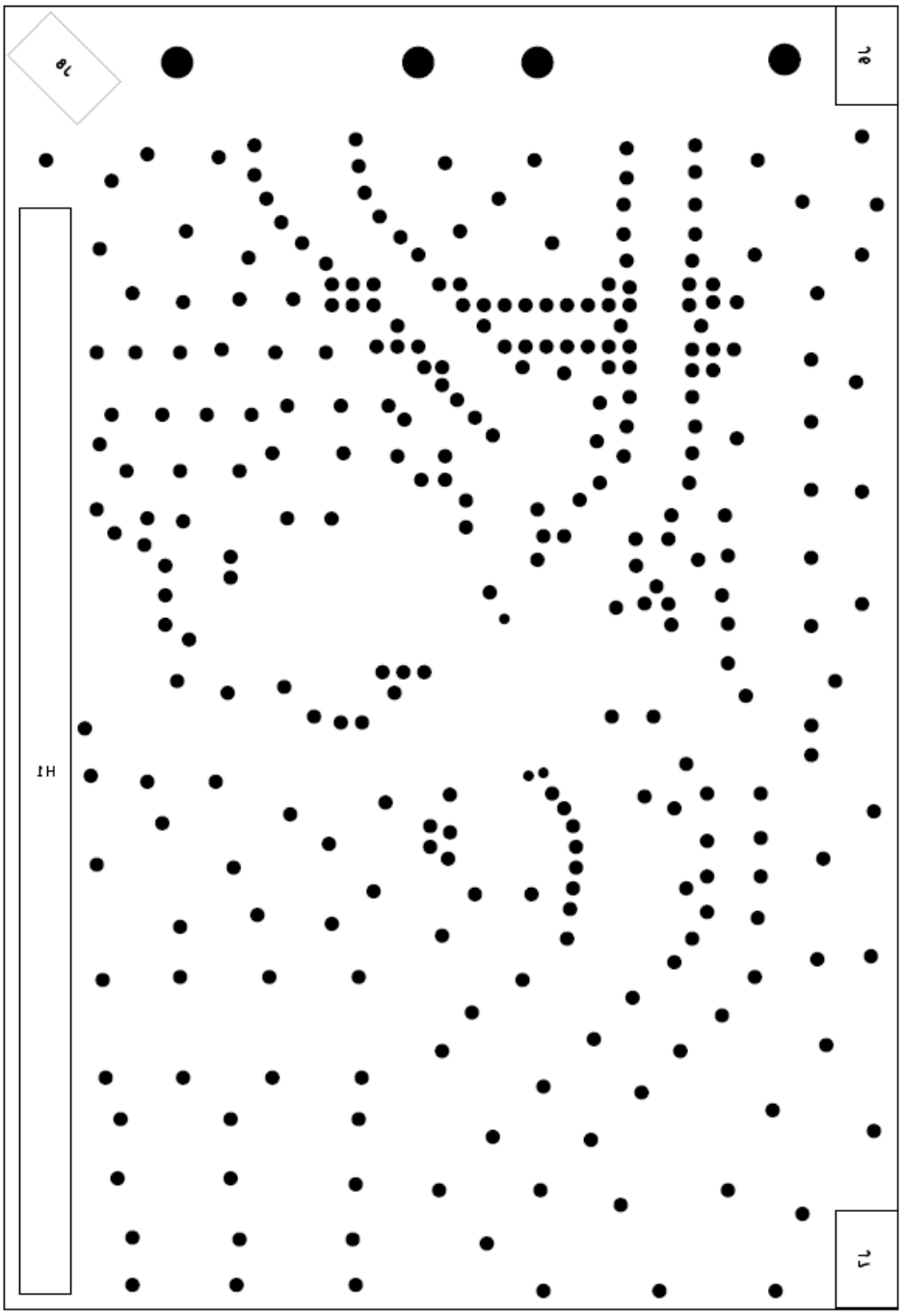

Figure 11 – MxL201RF component placement bottom layer

7. Gerber Reference Information

Gerber files of both 2-layer PCB and 4-layer PCBs are included in the MxL201RF hardware design guide. The Gerber files contain printed circuit board (PCB) layout and other files required for PCB fabrication. All Gerber files in the package are listed in Table 3 below.

File Name	Description
Bot.art	Copper mask on bottom layer
Top.art	Copper mask on top layer
Lyr2.art	Copper mask on 2nd layer (For 4-layer PCB only)
Lyr3.art	Copper mask on 3rd layer (For 4-layer PCB only)
Pastemasktp.art	Solder paste mask on top layer
Pastemaskbot.art	Solder paste mask on bottom layer
Masktop.art	Soldermask on top layer
Maskbot.art	Soldermask on bottom layer
Fab.art	A fabrication diagram
NCDRILL.drl	Drill coordinates file
Assemblytop.art	An assembly diagram for the top layer
Assemblybot.art	An assembly diagram for the bottom layer

Table 3 – List of Gerber references

These Gerber files were created on a 62 mil thickness PCB board. The dielectric material used is FR-4 and the copper weight is 1 oz. The PCB stack-up of both 2-layer PCB and 4-layer PCB is shown in Figure 12 and Figure 13. All Gerber files were created according to RS274X format. As mentioned in the layout guidelines section, for PCBs with different stack-ups the width of RF input trace needs to be adjusted so that the characteristic impedance of RF input trace is exactly 75Ω.

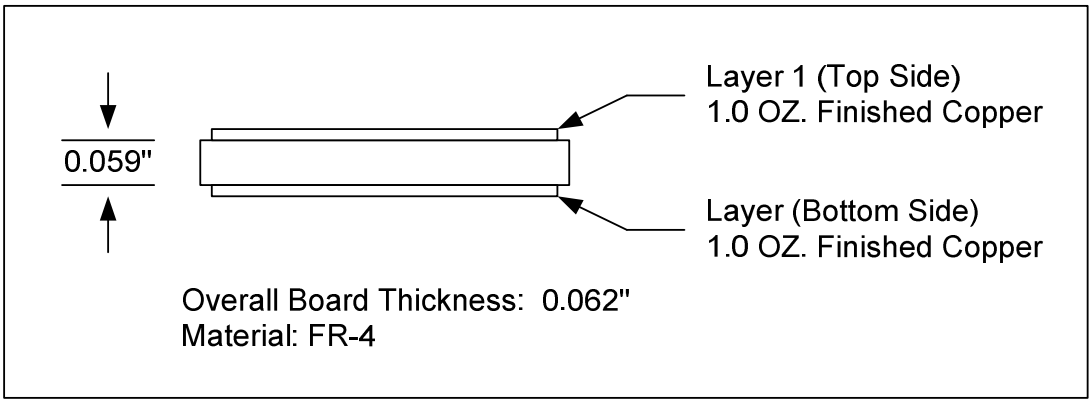

Figure 12 – Stack-up of 2-layer PCB

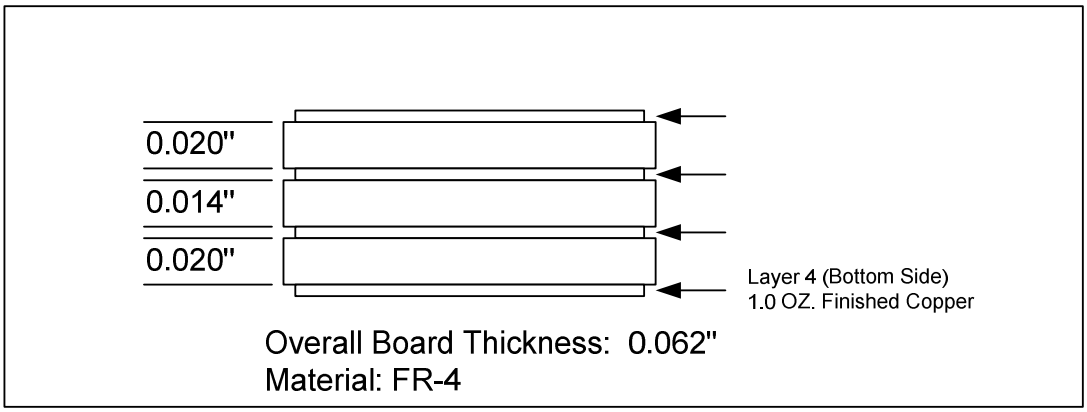

Figure 13 – Stack-up of 4-layer PCB

8. Revision History

Rev 4.0, April 22, 2009

1. First release of MxL201RF tuner reference design document Rev 4.0

Rev 4.1, May 18, 2009

1. Added ESD protection diode for loop-through path

Rev 5.0, July 21, 2009

1. Removed ferrite beads on supplies VBATT_A1 and VBATT_A2
2. Added PCB layout guidelines as section 5

Rev 5.1, February 18, 2010

1. Added optional Wi-Fi filter.
2. Updated BOM list.

Rev 5.2, August 27, 2010

1. Removed ferrite beads on supplies Vdd_A1.6V_D (Pin 19), VBATT_A3 (Pin 4) and VDD_DNX1 (Pin 31, Tracking Filter Sections). Shared ferrite bead between VDD_DNX1 and VDD_DNX2 (Pin 1).
2. Updated BOM list.