

DR78316M-V3.01

Turnkey

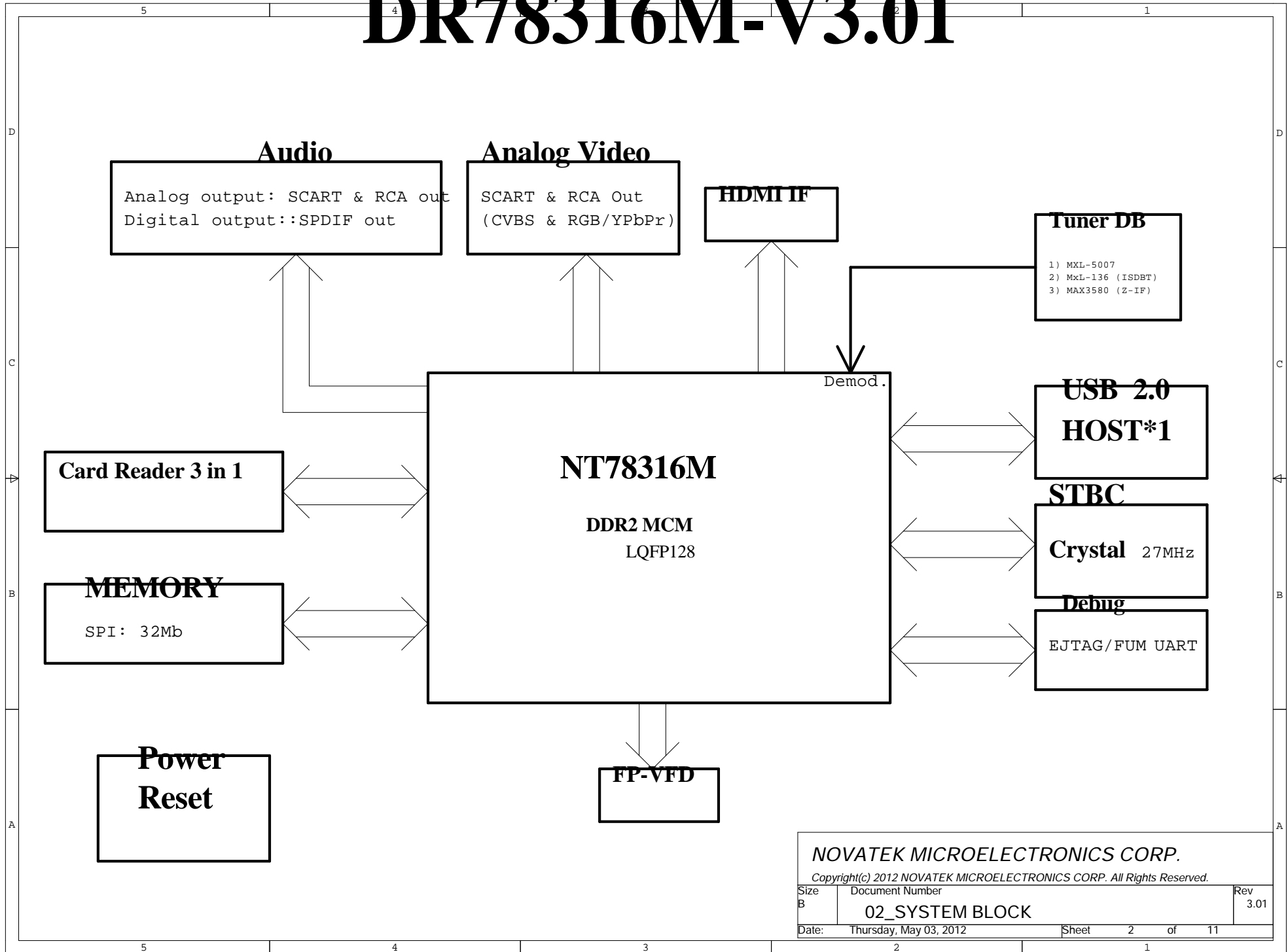
REVISION TABLE

Date	Schematic	Layout	Change notice
2012/02/06	V3.0	V3.0	1st draw
2012/04/30	V3.01	V3.01	2nd draw

第 1 版 図 面 等 の 誤 差 等 による 誤 差 等 の 発生 防止 ため 本 図 面 等 の 再 考 査 等 を 行 っ た こと を 記 載 する こと と し ます 。
 ESD, EMC/EMI 単 独 の 図 面 等 による 誤 差 等 の 発生 防止 ため 本 図 面 等 の 再 考 査 等 を 行 っ た こと を 記 載 する こと と し ます 。
 本 図 面 等 の 再 考 査 等 を 行 っ た こと を 記 載 する こと と し ます 。

This declaration is made by Novatek Microelectronics Corp. "Novatek" to declare that the design documents and any other related documents provided by Novatek are solely for our customers' internal reference. Due to the discrepancies among the application circuit, PCB material, layout, component and mechanism which shall influence safety of power, power consumption, system performance, temperature, ESD, EMC/EMI and so on, for the avoidance of the dispute in the future, Novatek officially uses this declaration to disclaim the warranty of the documents provided by Novatek as set forth herein will apply to all application and MP specification. Furthermore, Novatek suggests that all customers shall refer to all documents provided by Novatek particularly prior to the development, in case any customer needs Novatek's assistance with respect to such documents, please doesn't hesitate to contact with the related contact windows of Novatek.

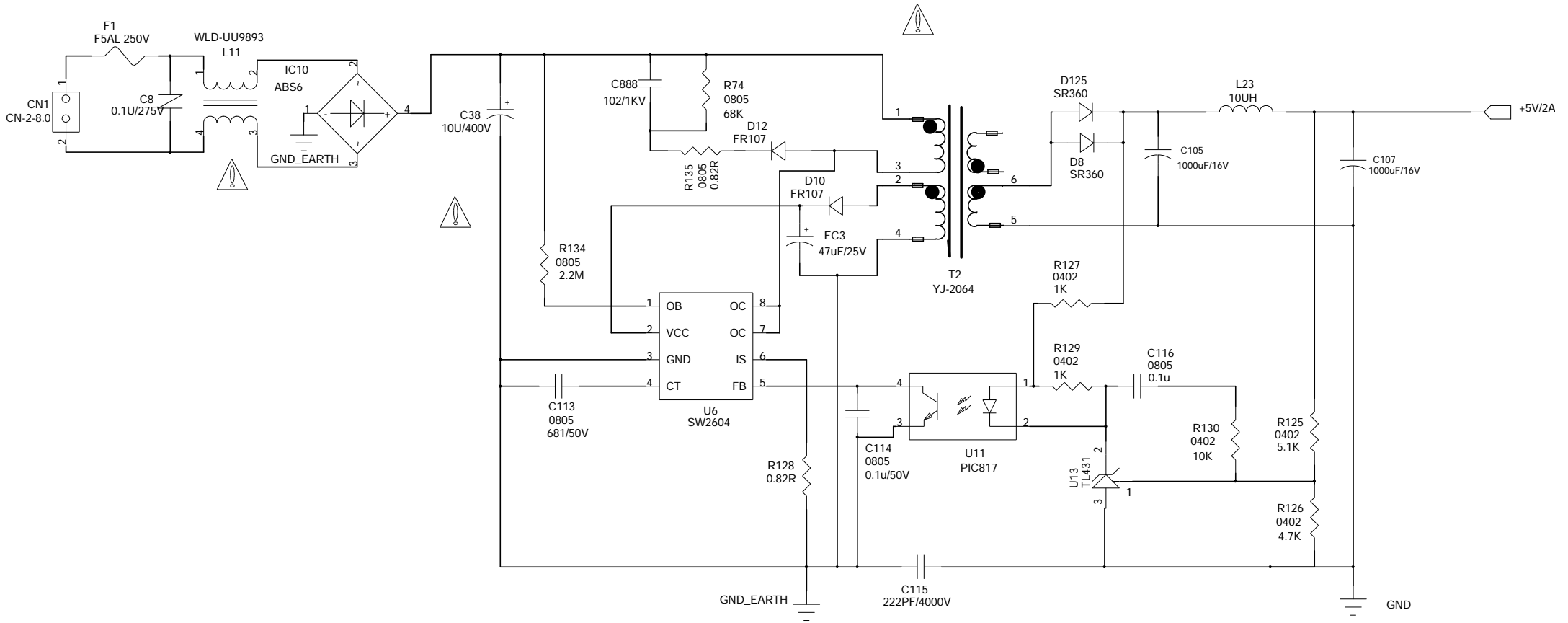
DR78316M-V3.01

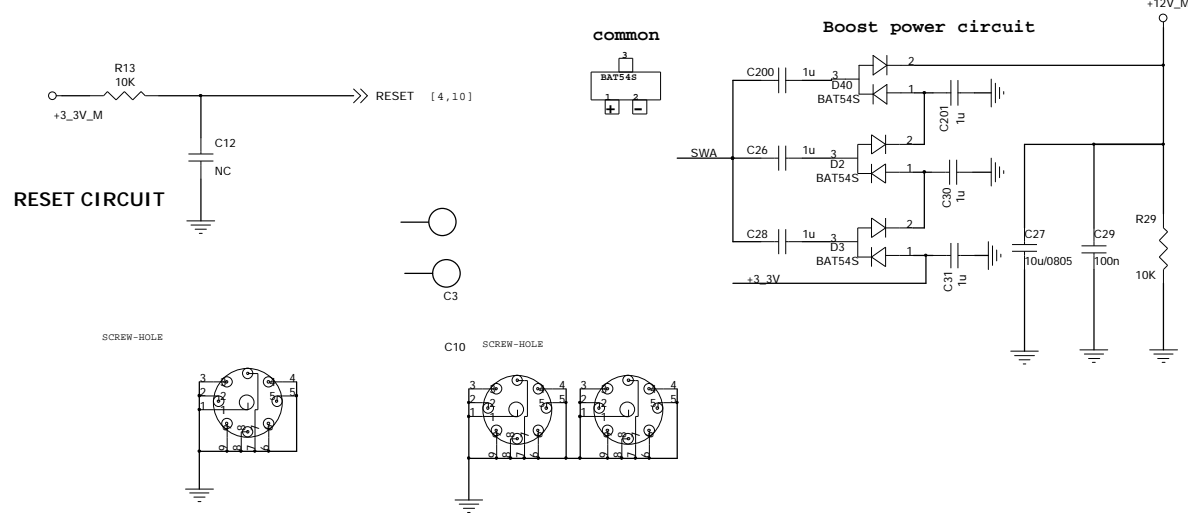
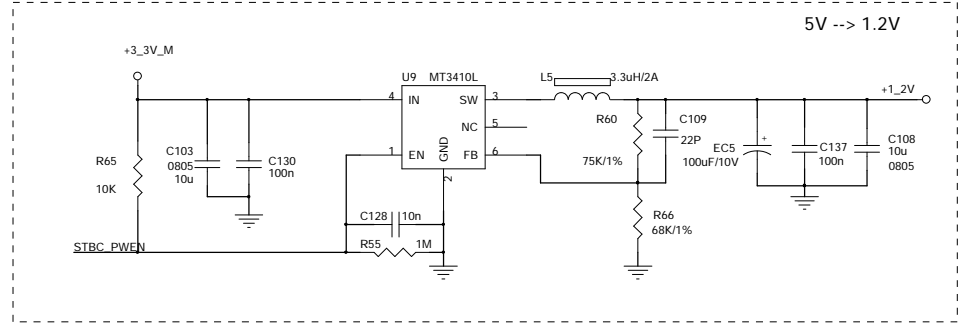
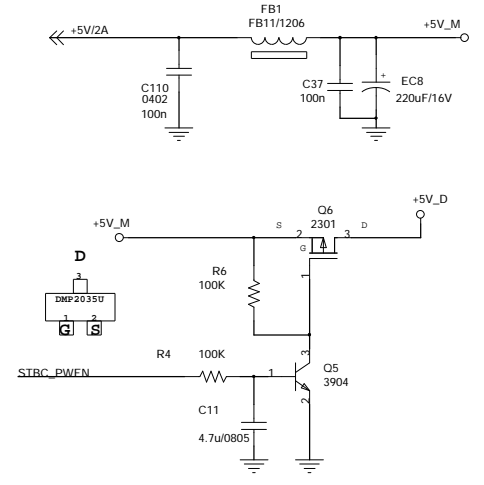
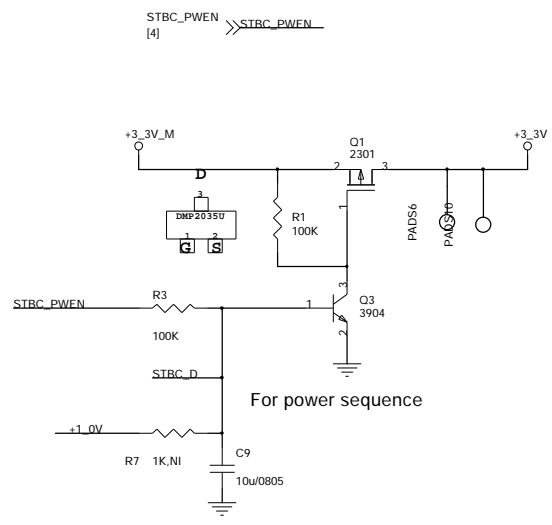
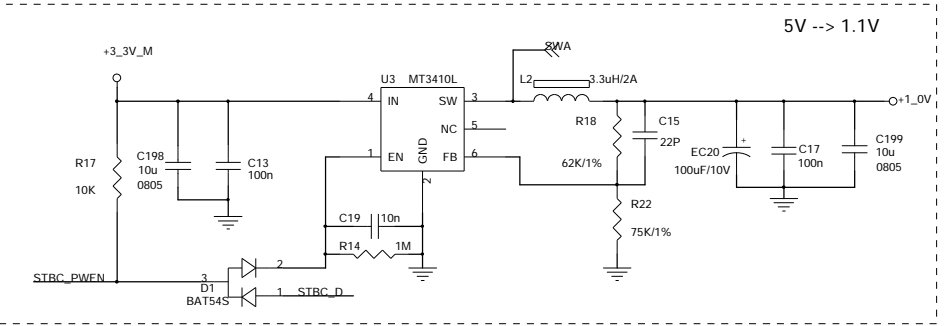
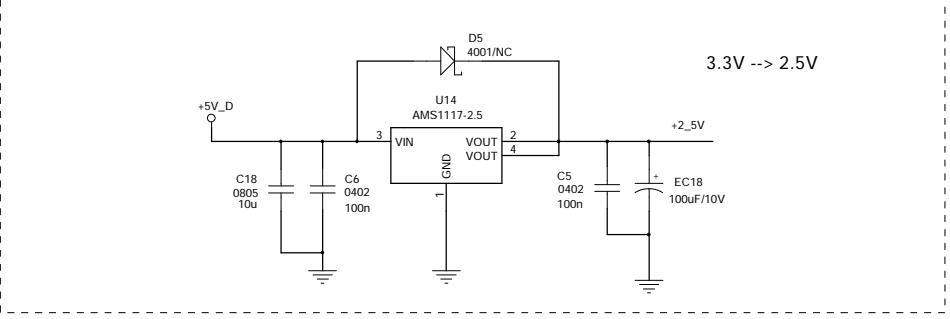
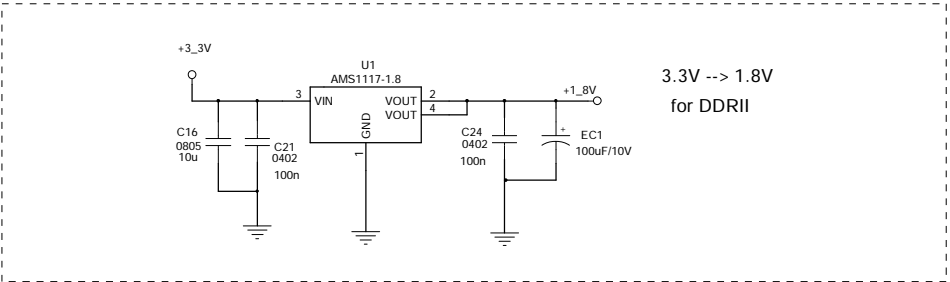
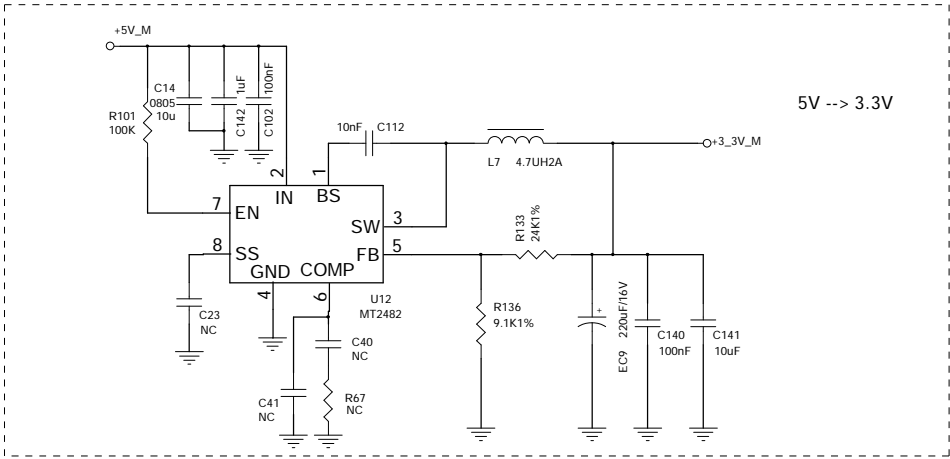


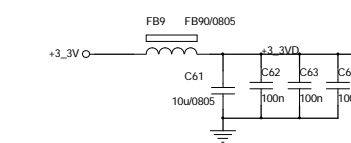
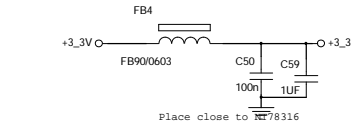
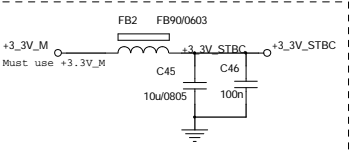
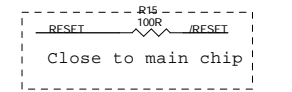
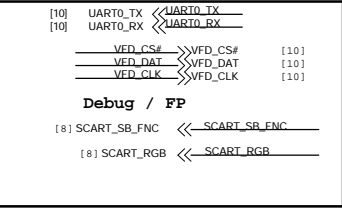
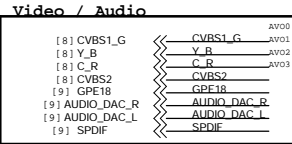
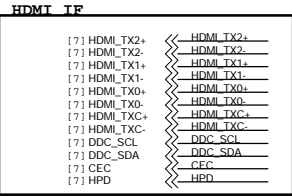
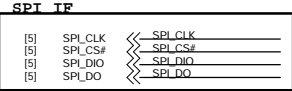
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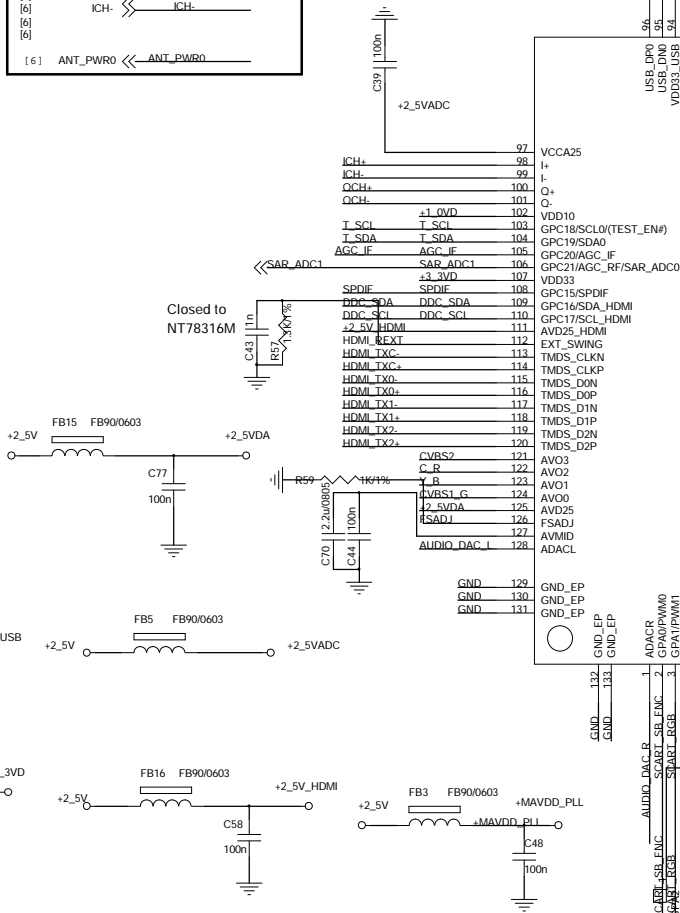
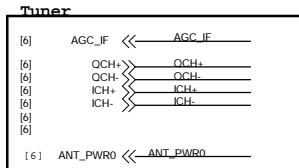
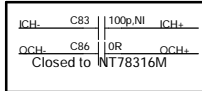
Size B	Document Number 02_SYSTEM BLOCK	Rev 3.01
Date: Thursday, May 03, 2012	Sheet 2	of 11





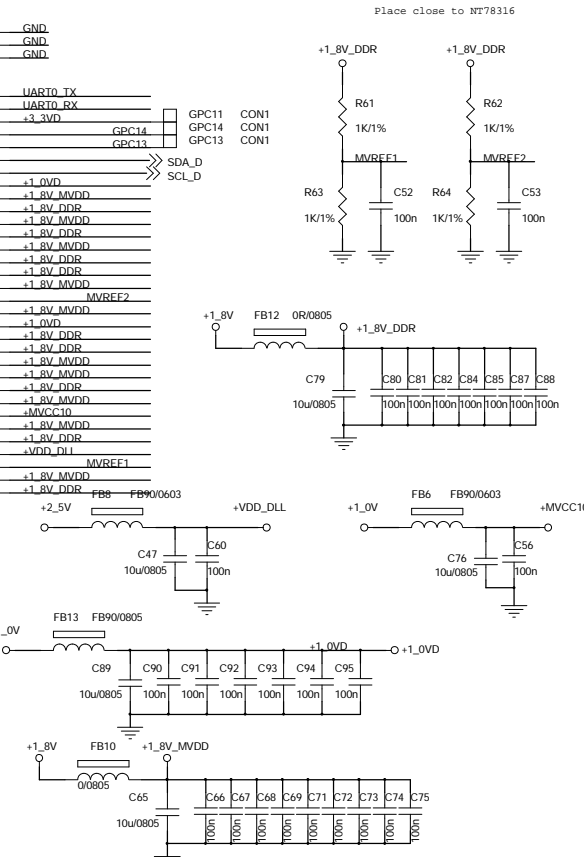
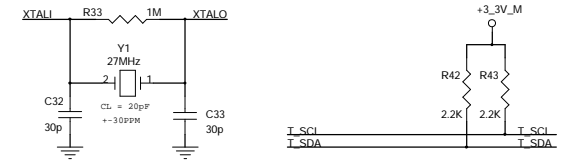


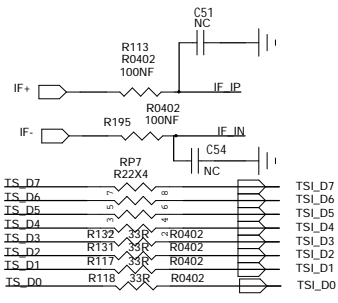
NT78316M can support Zero-IF input.
If Low/Direct IF is used, please keep the other channel always OPEN.



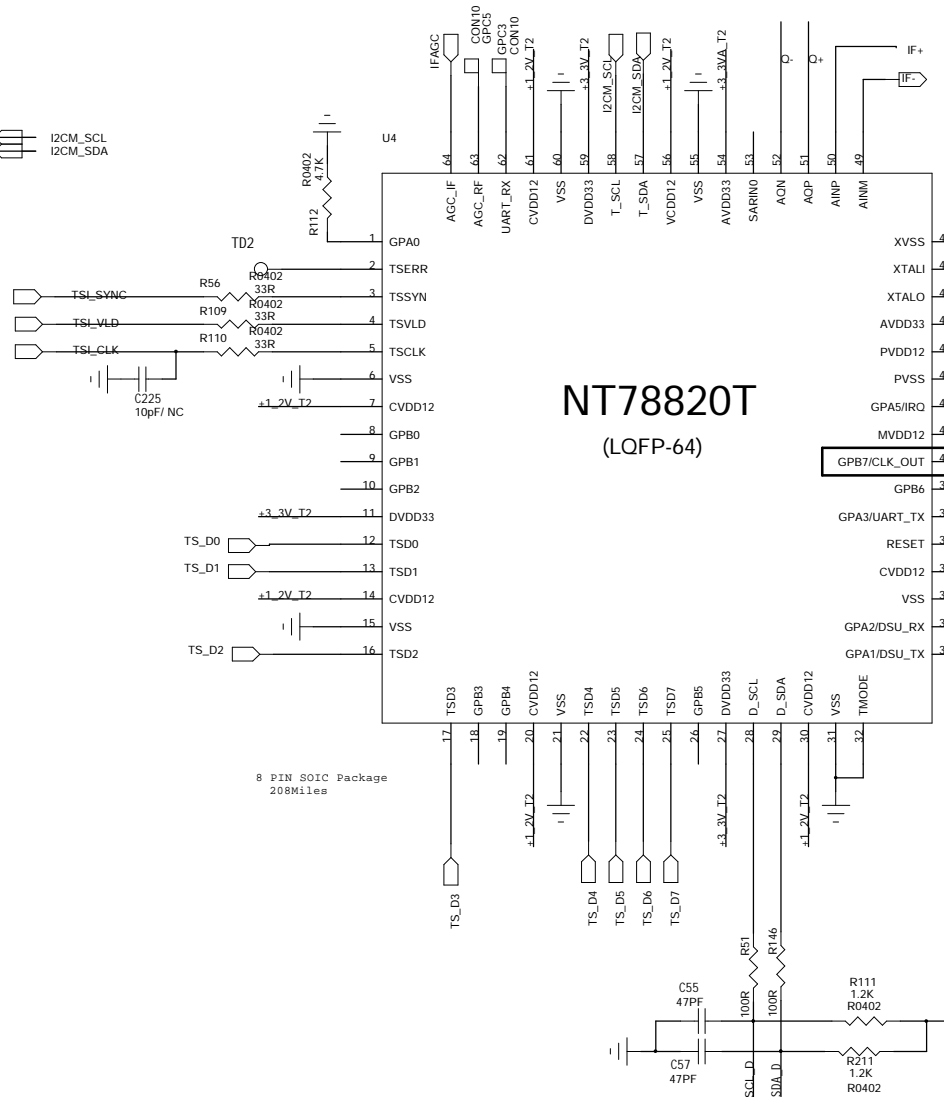
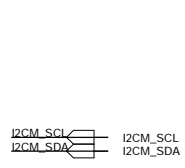
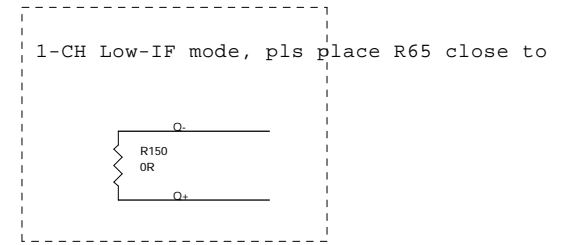
Power On Configuration(POC) Setting

Pin	Value	Defintion	Default
(GPA4)	1	Boot from ROM	V
	0	Boot from SPT	
(GPE14)	1	Normal power-on reset (250ms)	V
	0	Fast reset mode for test	
(GPC18)	1	Normal run	V
	0	Test mode enable	



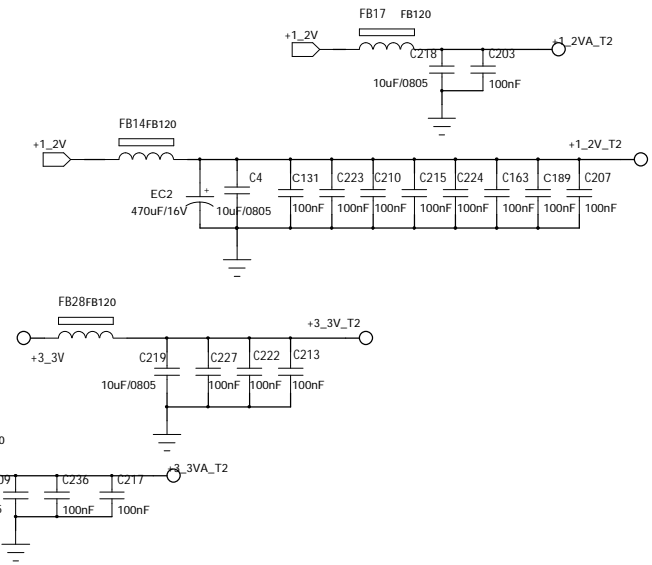


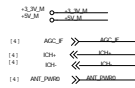
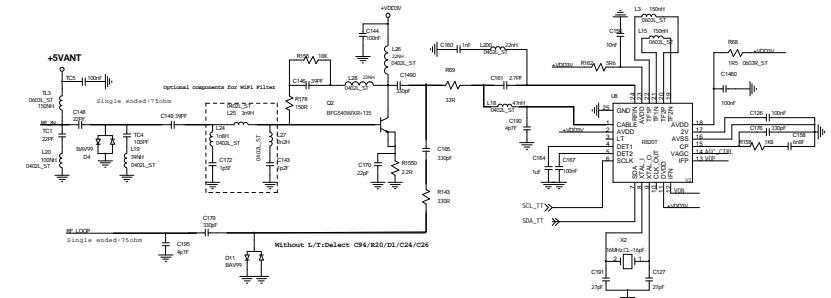
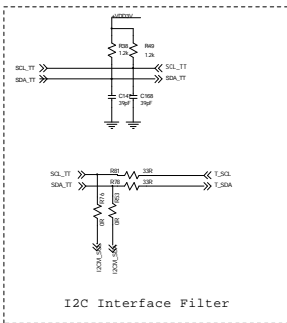
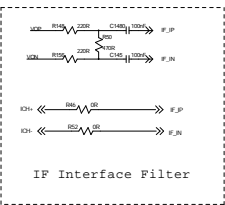
BPF Reserved



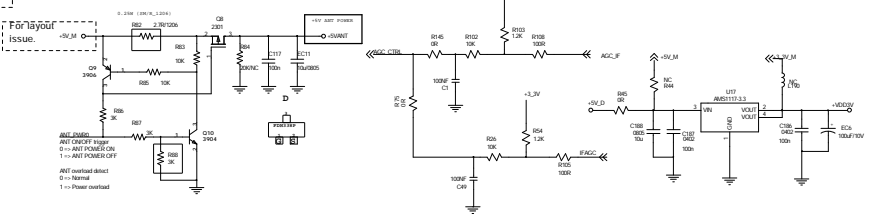
NT78820T
(LQFP-64)

8 PIN SOIC Package
208Miles



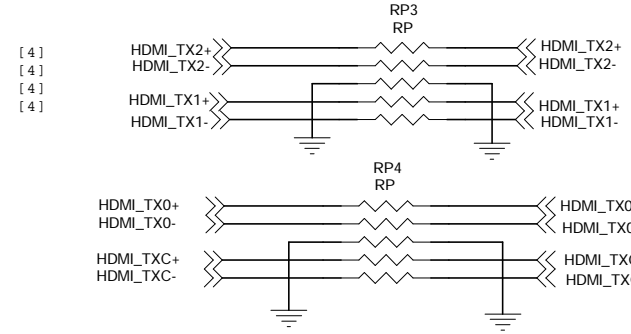
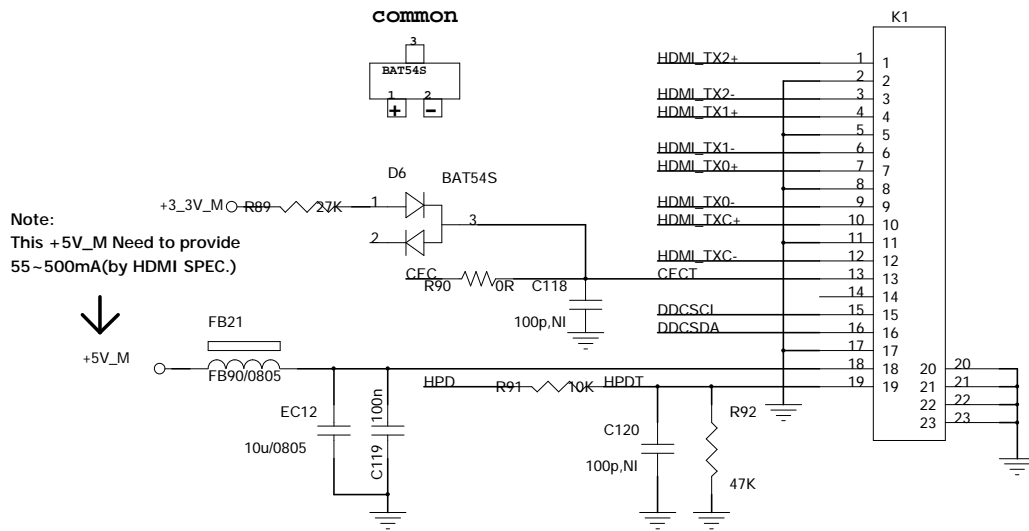


+VDD3V
 -VDD3V
 +VDD3V Input Ripple must be under 10mVp-p



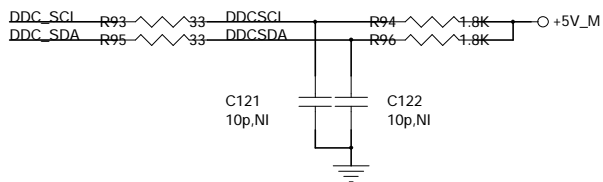
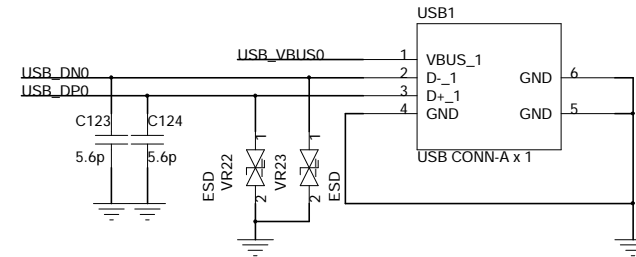
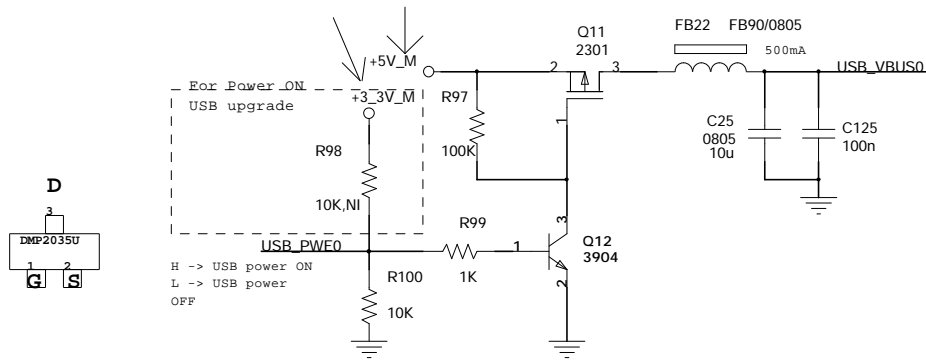


HDMI IF



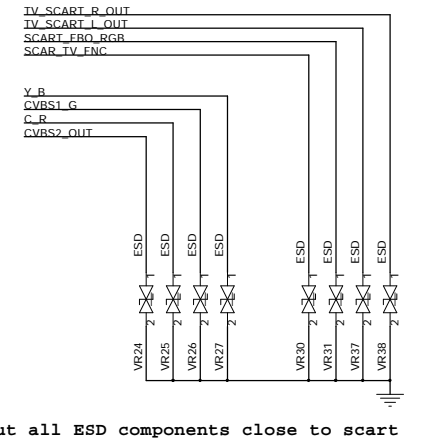
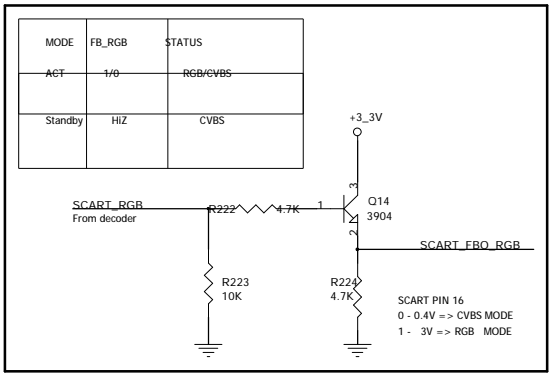
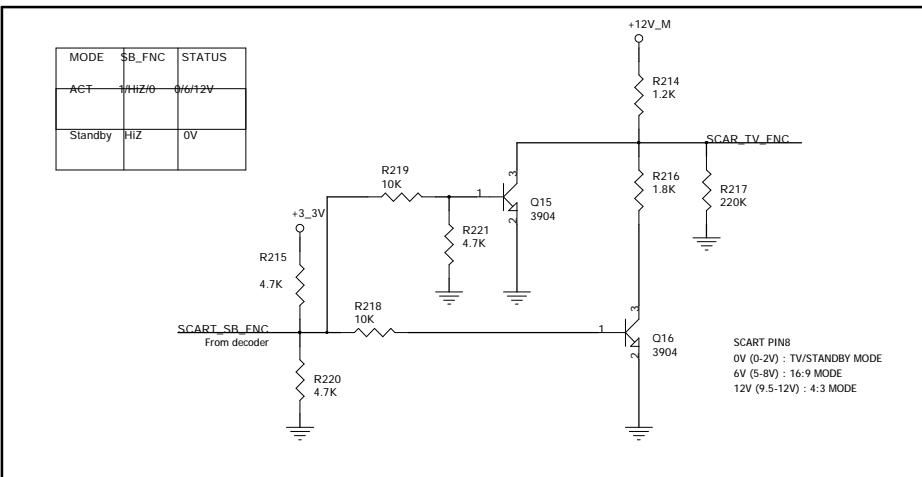
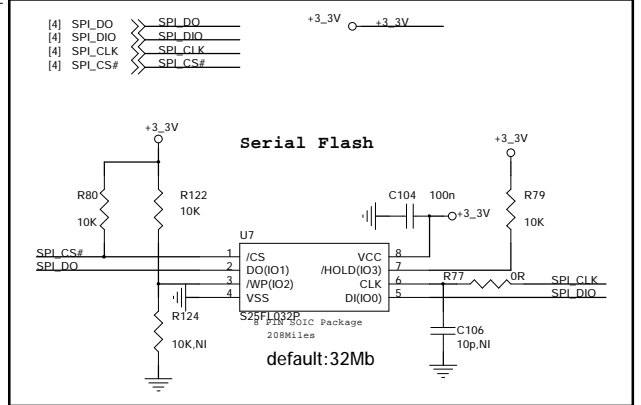
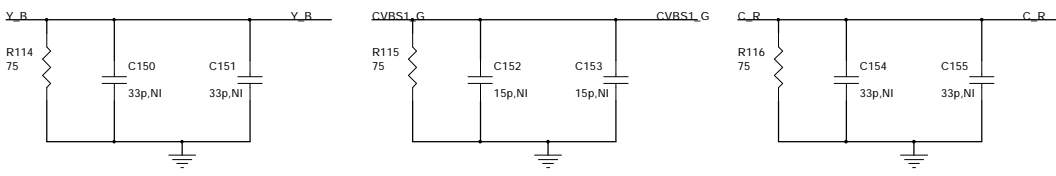
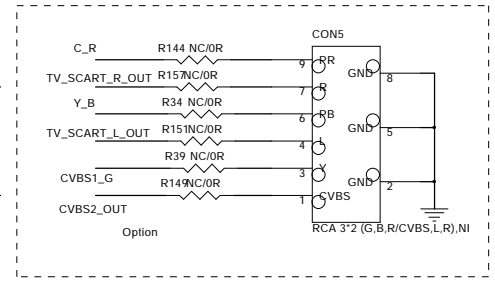
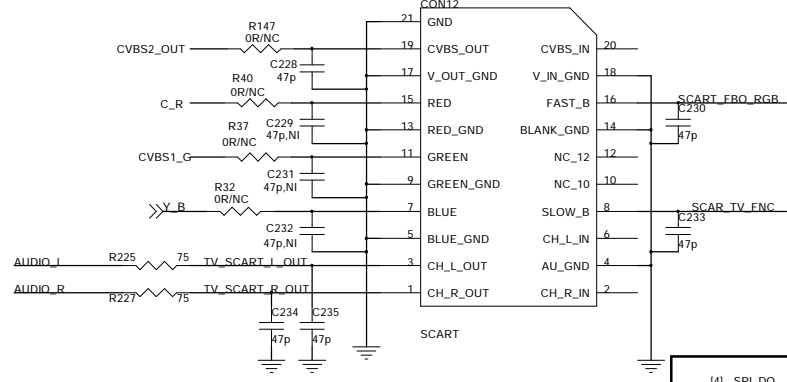
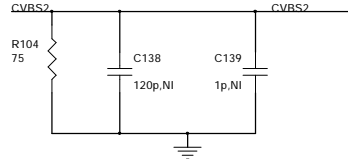
Put all ESD components close to the I/O connector

For layout issue

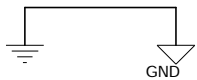
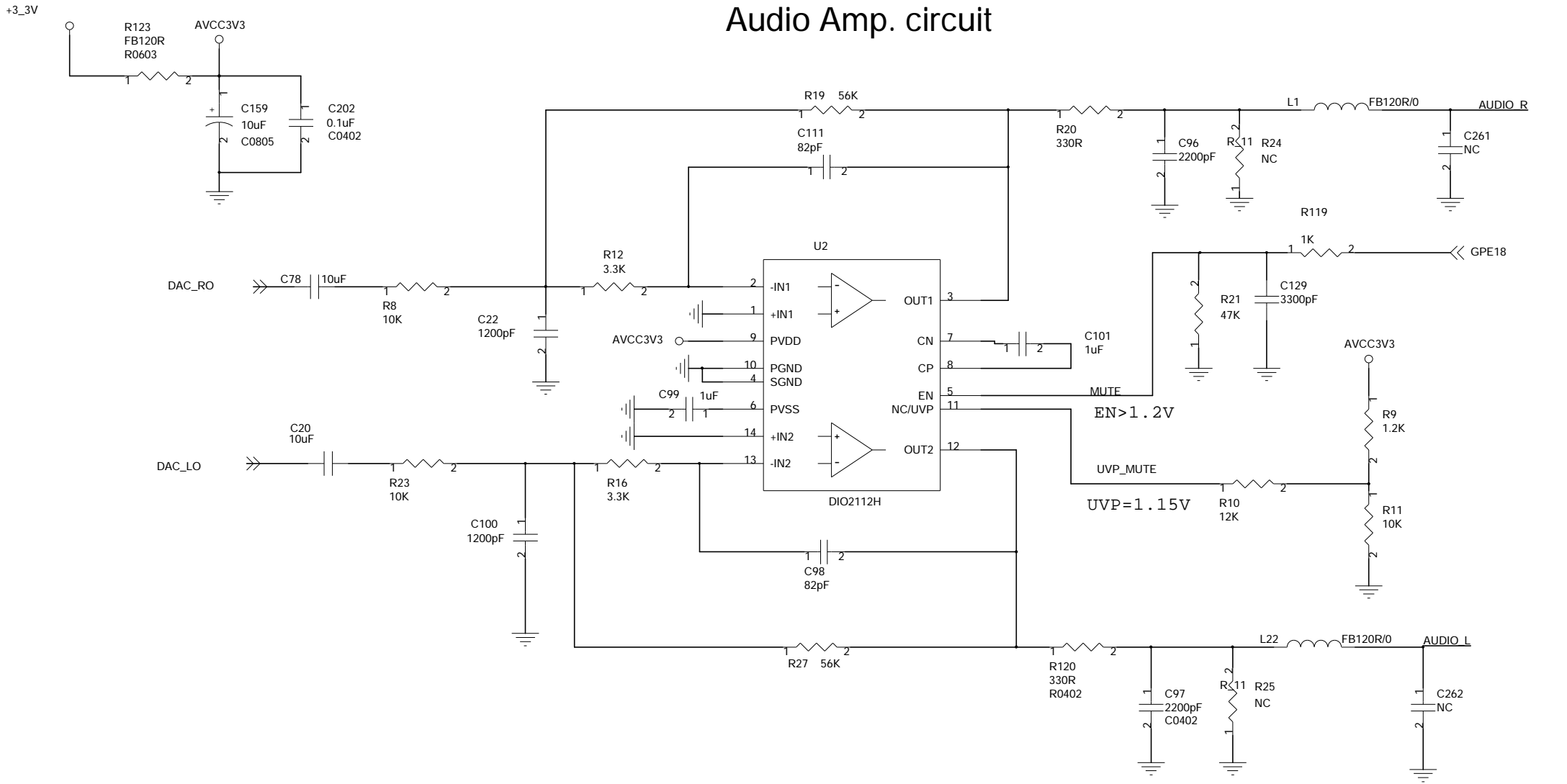


TV_SCART

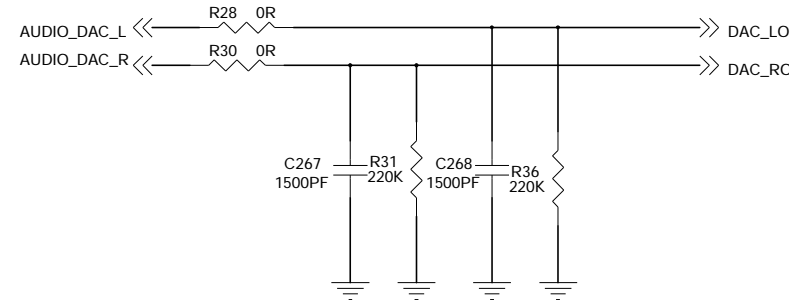
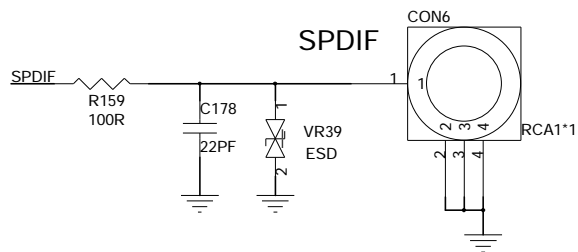
- [4] SCART_RGB >> SCART_RGB
- [4] SCART_SB_FNC >> SCART_SB_FNC
- [4] CVBS1_G >> CVBS1_G
- [4] Y_B >> Y_B
- [4] C_R >> C_R
- [4] CVBS2 >> CVBS2
- [9] AUDIO_R >> AUDIO_R
- [9] AUDIO_L >> AUDIO_L



Audio Amp. circuit

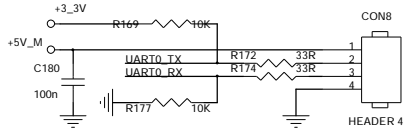


- [8] AUDIO_R << AUDIO_R
- [8] AUDIO_L << AUDIO_L
- [4] AUDIO_DAC_R << AUDIO_DAC_R
- [4] AUDIO_DAC_L << AUDIO_DAC_L
- [4] SPDIF << SPDIF
- [4] GPE18 << GPE18



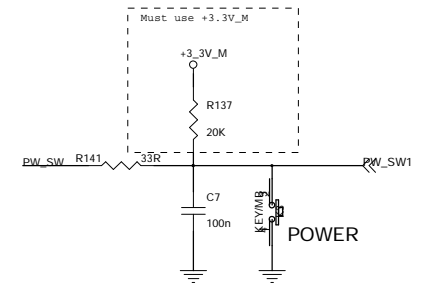
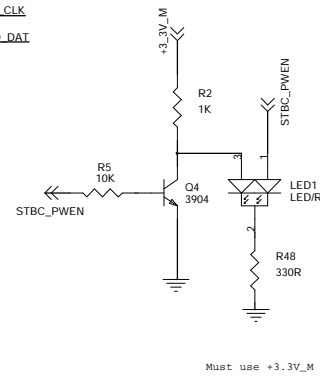
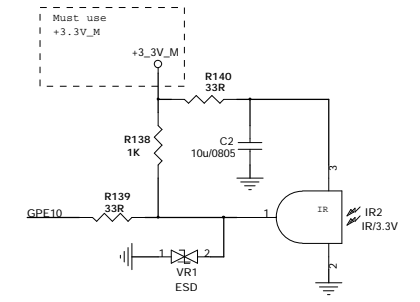
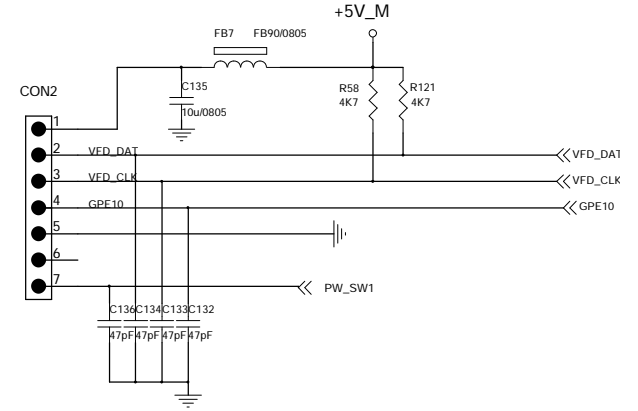
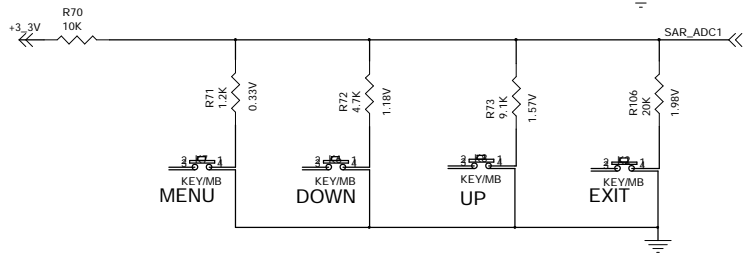
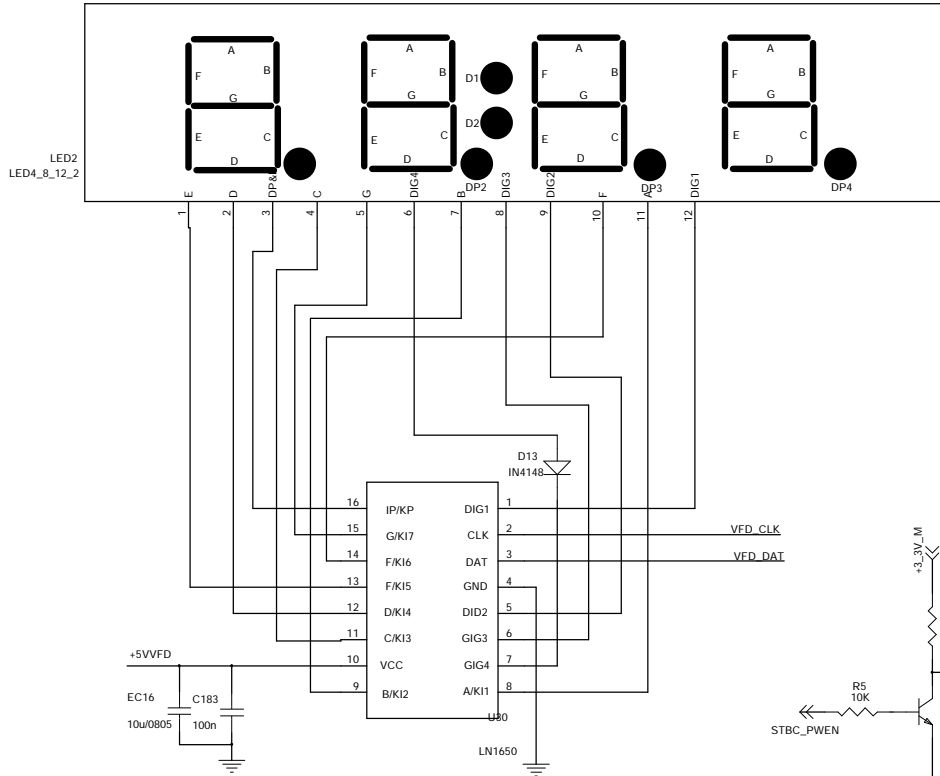
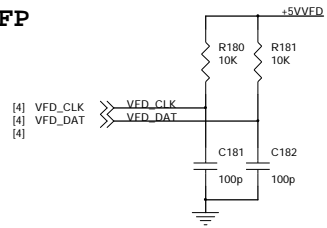
For layout issue UART0

[4] UART0_TX << UART0_TX
 [4] UART0_RX << UART0_RX



+5V_M L14 FB90/0603 +5VVFD

FP



STBC_PWEN:
 H:Action mode; STBYLED OFF
 L:Standby mode; STBYLED-ON