NMI120 Datasheet

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Revision 3.3

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Revision History

Revision Number	Date	Modified by	Comments
1.0	Nov-1-2010	Janakan Siva	Preliminary version for release
2.0	Jan-27-2011	Janakan Siva	Removed 20-pin package information Modified 16-pin package information
2.1	Feb-12-2011	Janakan Siva	Updated Specs
3.0	Jul-4-2011	Janakan Siva	Removed 3x3mm package information Added 4x4mm package information Updated specifications with production silicon data
3.1	Jul-8-2011	Janakan Siva	Corrected typo in package thickness and pad dimensions
3.2	Jul-20-2011	Janakan Siva	Updated pin-out and I2C Address select info
3.3	Jul-29-2011	Janakan Siva	Updated pin-out and I2C Address select info

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1 Introduction

The NMI120 is a digital terrestrial television tuner. Leveraging NMI's proprietary tuner IP, it simultaneously delivers best-in-class form factor, BOM, power consumption, and performance. It is ideal for STB (set top box) and Television applications and supports DVB-T, ATSC, ISDBT-13seg, and DTMB.

1.1 Key Features

- Cost-effective 4x4mm QFN package
- Ultra low current consumption: 145mA typical, half of competitors
- Lowest BOM: no SAW, balun, or tracking filter required.
- Significant margin to NorDig, D-book, A/74, ARIB, and GB20600 standards.
- 4.0dB NF and up to +20 dBm IIP_3
- Integrated low noise loop through and crystal oscillator buffers for efficient multi-tuner support.
- Single1.8-3.3V IO supply with integrated power management circuitry.
- Adjustable IF output frequency (3 – 60 MHz) facilitates interface with various digital demodulators.
- Fully integrated VCOs, PLL loop filter, and crystal oscillator
- I^2C control interface
- Environmental Compliance: NMI120 is Pb-free, Cd-free, Halogen free and RoHS compliant

1.2 Applications

- Digital Terrestrial Television STB
- LCD, PDP, and CRT Television
- Automotive TV Tuners
- Portable TVs and DVD players
- Laptop Computers
- Cell Phones and PDAs

1.3 Description

The NMI120 takes a single-ended RF input signal from the antenna and passes it through a wideband RF front-end that processes signals from 44 to 862 MHz. It supports VHF-I, VHF-III, and UHF-bands. The tuner integrates the LNAs, mixers, VCO, PLL/loop filter, LO generation, crystal oscillator, baseband filters and amplifiers. External baluns, SAW filters, and tracking filters are not required. The tuner also includes innovative, fully integrated RF and IF gain control loops.

The NMI120 requires only a single, flexible 1.8-3.3V supply for operation. Integrated power management circuitry generates a 1.2V supply for internal usage. In multi-tuner scenarios, the integrated loop through and crystal oscillator buffers allow for low cost and scalability. The fully integrated low-noise loop through buffer, at 5dB NF typical, allows downstream tuners to have 3dB better sensitivity than existing solutions.

The NMI120 communicates with the host via I^2C, and outputs differential IF signals to a wide range of demodulators.

1.4 Block Diagram

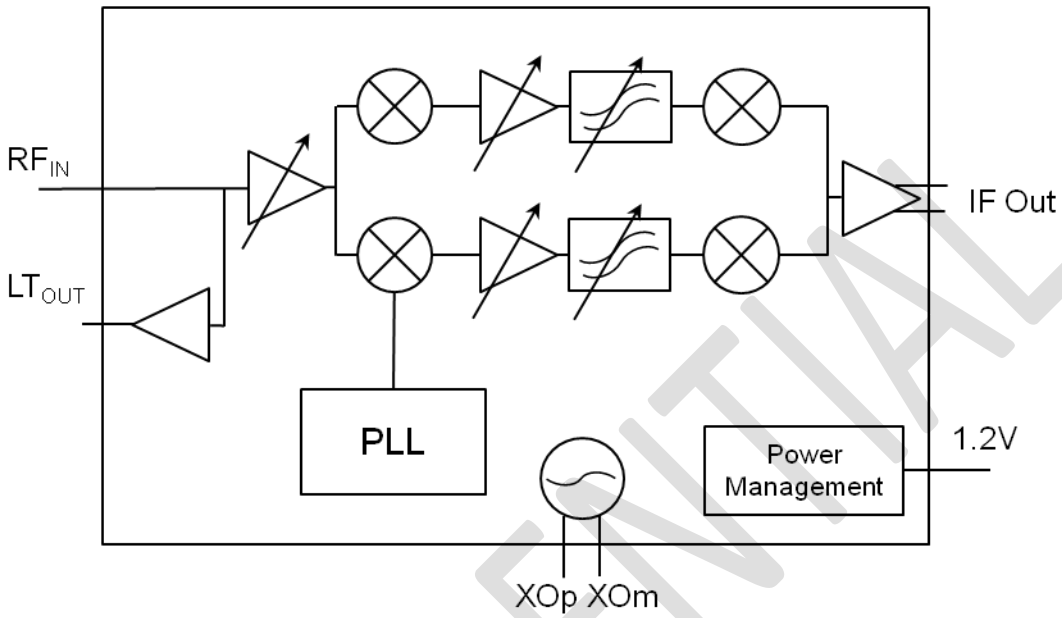

Figure 1: NMI120 Block Diagram

2 Electrical Specifications

2.1 Absolute Ratings

Table 1 provides the absolute ratings for NMI120. Stresses outside the limits listed in Table 1 may permanently damage the device. This is a stress rating only; functional operation of the device at these or any other conditions outside the limits listed in Table 2 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1: NMI120 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
1.2V Supply Voltage	VDD_1P2	-0.3	1.5	V
I/O Supply Voltage	VDDIO	-0.3	3.6	V
Digital Input Voltage	V_{IN}	-0.3	VDDIO +0.3 (up to 3.6)	V
Analog Input Voltage	V_{AIN}	-0.3	1.5	V
ESD Human Body Model	V_{ESDHBM}	-1000	+1000	V
Storage Temperature	T_A	-65	150	^oC
Junction Temperature			125	^oC
RF input power max			15	dBm

Notes:

V_{IN} rating applies to the following pins: I2C_SDA and I2C_SCL.

2.2 Recommended Operating Conditions

Table 2: NMI120 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Units
1.2V Supply Voltage	VDD_1P2	1.15V	1.2	1.3V	V
I/O Supply Voltage Low Range	$VDDIO_L$	1.75	1.80	1.9	V
I/O Supply Voltage High Range	$VDDIO_H$	3.00	3.30	3.60	V
Operating Temperature		-20		85	^oC

Notes:

For extended operating temperature range, including automotive or industrial grade, please contact your NMI representative

2.3 PAD DC Electrical Characteristics

Table 3 provides the DC characteristics for the NMI120 I^2C pads.

Table 3: NMI120 DC Electrical Characteristics

VDDIO Condition	Characteristic	Min	Max	Unit
$VDDIO_L$	Input Low Voltage V_{IL}	-0.30	0.63	V
	Input High Voltage V_{IH}	1.17	VDDIO+0.30	V
	Output Low Voltage V_{OL}		0.30	V
	Output High Voltage V_{OH}	VDDIO-0.22		V
$VDDIO_M$	Input Low Voltage V_{IL}	-0.30	0.70	V
	Input High Voltage V_{IH}	1.70	VDDIO+0.30	V
	Output Low Voltage V_{OL}		0.20	V
	Output High Voltage V_{OH}	VDDIO-0.14		V
$VDDIO_H$	Input Low Voltage V_{IL}	-0.30	0.80	V
	Input High Voltage V_{IH}	2.00	VDDIO+0.30 (up to 3.60)	V
	Output Low Voltage V_{OL}		0.16	V
	Output High Voltage V_{OH}	VDDIO-0.11		V
All	Output Loading		20	pF
All	Digital Input Load		6	pF

The guarantees for output low voltage, V_{OL}, and output high voltage, V_{OH}, assumes 1mA drive current for low drive pads and 2mA drive current for high drive pads across process and temperature.

2.4 Crystal Oscillator

Table 4: NMI120 Crystal Oscillator Parameters

Parameter	Min	Typ	Max	Units
Crystal Resonant Frequency	12		40	MHz
Crystal Equivalent Series Resistance		50	150	Ω
Stability	-70		+70	ppm

The block diagram in Figure 2 shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5pF internal capacitance on each terminal XO_P and XO_N.

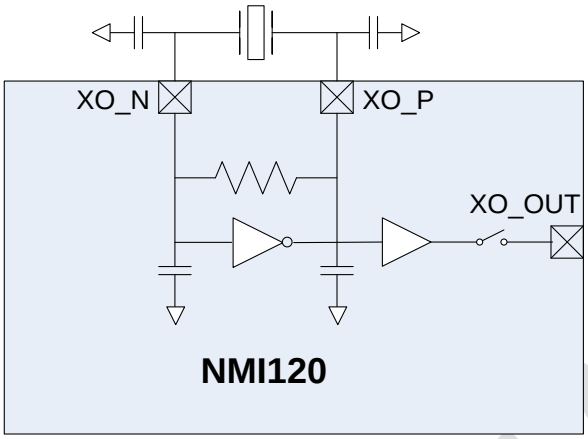

Figure 2: NMI120 XO connections to crystal

Table 5 specifies the electrical and performance requirements when an external clock source is used.

Table 5: NMI120 Bypass Clock Specification

Parameter	Conditions	Min	Max	Unit	Comments
Oscillation frequency		12	40	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing		0.3	1.5	V_{pp}	AC coupled input
Phase Noise	At 1KHz offset		-120	dBc/Hz	
Jitter (RMS)			<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

2.5 Tuner AC Characteristics

Table 6: AC Characteristics

Parameter	Min	Typ	Max	Units	Comments
Frequency Range	44		862	MHz	Covers VHF I,III and UHF terrestrial
S_{11}	-6	-10		dB	
Tuner Gain Range	-20		100	dB	
Supply Voltage Ripple			10	mV	Peak-to-peak voltage
Active Current		145		mA	Loop Through disabled
Noise Figure		4.0	6.0	dB	
IIP_3 (Min Gain)		20		dBm	

IIP_3 (Max Gain)		-5		dBm	N+8, N+16 blockers
IIP_2 (Min Gain)		40		dBm	
IIP_2 (Max Gain)		20		dBm	N+8, N+16 blockers
LO integrated Phase Noise		0.8		°	
Image Rejection		65		dBc	Across channel band.
IF Blocks					
Channel Bandwidth	6		8	MHz	Programmable
Channel Filter Stopband Attenuation		75		dBc	
Total Group Delay		275		ns	
IF Frequency	3		60	MHz	Fully programmable in this range
Digital IF Output Swing		1		Vpp	Differential p-p swing at IF.
Loop Through Buffer					
Loop Through Gain	-2		+2	dB	Gain is programmable.
Loop Through Output Impedance		75		Ω	
Loop Through Noise Figure		5		dB	
Loop Through Current		30		mA	

3 Pin-Out and Package Information

3.1 24-pin 0.5mm pitch QFN Pin-Out and Package Information

The NMI120 is offered in a 0.5mm pitch 24-pin 4x4mm QFN with exposed pad. The QFN pin connectivity is described in Table 7 below – the pins are described from the left hand side of the chip counter-clockwise.

Table 7: NMI120 24-pin QFN Pin Connectivity

Pin #	Name	Description
1	Chip Ena	Chip Enable (VDD_IO)
2	VDD_1p8	Internal 1.8V Supply Decoupling
3	RF IN	42-862MHz RF input
4	LT out	Loop Through
5	VDD RF	1.2V RF Supply
6	NC	No Connect
7	NC	No Connect
8	SCL	I^2C Clock
9	SDA	I^2C Data
10	XO_buf_out	Crystal Oscillator Buffer out
11	VDD Anlg	1.2V Analog Supply
12	NC	No Connect
13	NC	No Connect
14	IF_out_n	Differential IF output, minus
15	IF_out_p	Differential IF output, plus
16	NC	No Connect
17	NC	No Connect
18	NC	No Connect
19	NC	No Connect
20	VDD_IO	IO VDD (1.8-3.3V)
21	XO_n	Negative Crystal Terminal
22	XO_p	Positive Crystal Terminal
23	LDO_out	1.2V LDO output
24	NC	No Connect
25	PAD	Exposed Pad, must tie to ground

The NMI120 24-pin 0.5mm pitch QFN pin map is shown in Figure 3. The exposed die pad (pin 25 in the Figure) must be tied to ground.

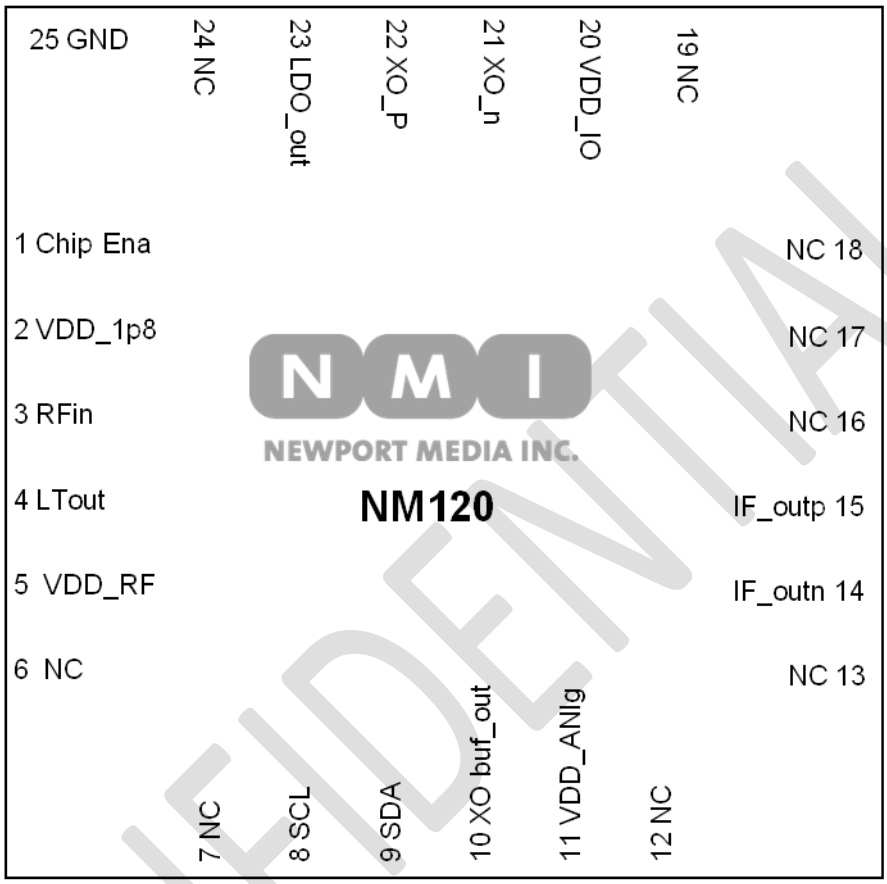

Figure 3: 24-pin 0.5mm pitch QFN Pin-Out

The NMI120 24-pin 0.5mm pitch QFN package information is provided in Table 98

Table 8: NMI120 24-pin 0.5mm pitch QFN Package Information

Parameter	Value	Units	Tolerance
Package Size	4 x 4	mm	+/- 0.1 mm
QFN Pin Count	24	Pins	
Total Thickness	0.85	mm	+ / - 0.05mm
QFN Pad Pitch	0.50	mm	
Pad Width	0.25	mm	
Exposed Pad Size	2.6	mm	

The NMI120 24-pin 0.5mm pitch QFN package outline is shown in Figures 4 and 5. The exposed die pad must be tied to ground.

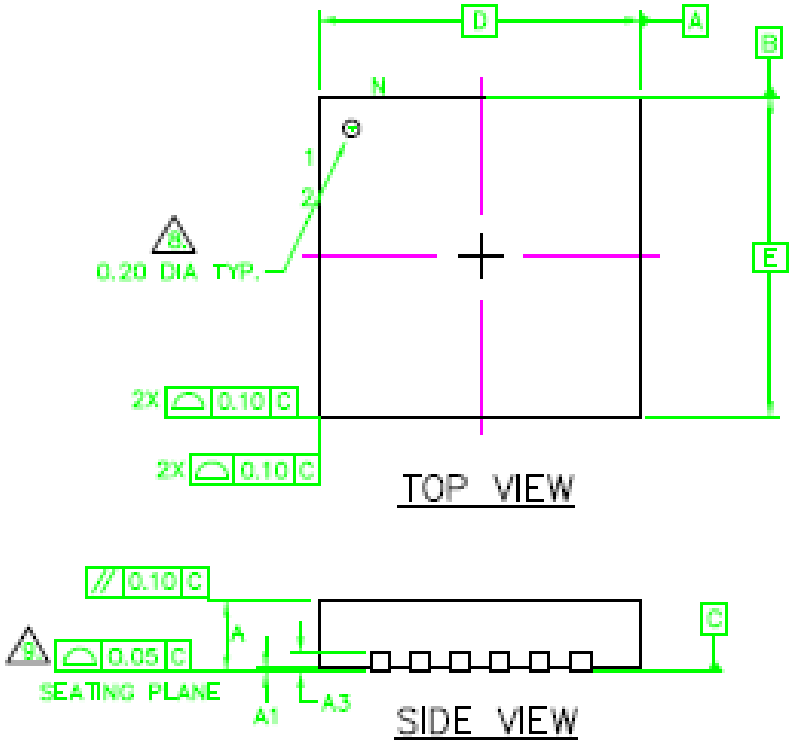

Figure 4: NMI120 24-pin Top & Side View

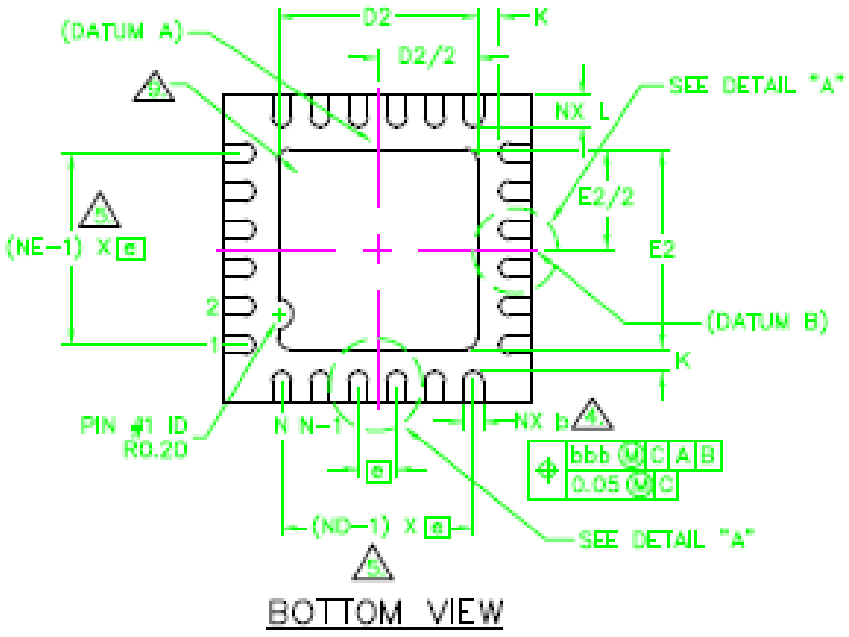

Figure 5: NMI120 24-pin Bottom View

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO–220
11. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (L1) MAYBE PRESENT
12. PULLBACK DESIGN OPTION IS FOR 0.50mm NOMINAL LANDLENGTH ONLY.

SYMBOL	VARIATION E		
	MIN.	NOM.	MAX.
e		0.50 BSC.	
N		24	
ND		6	
NE		6	
L	0.35	0.40	0.45
b	0.18	0.25	0.30
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
θ	0	——	12	2
K		0.20 MIN.		
D		4.0 BSC		
E		4.0 BSC		
L1		0.15 mm MAX		11

3.2 Package Qualification

The QFN package is qualified as Green Packages at the supplier. Newport Media Inc. packages comply with the most recent JEDEC J-STD-020 specification for peak reflow temperature requirements. The QFN package is qualified to the following conditions shown in Table 9. No delamination and no open-short failures were found after long-term reliability with Level 2 preconditioning with three times 260°C reflow.

Table 9: Summary of NMI120 QFN Package Level Qualification

Test	Test Condition	Reflow / Read Point
Pre-Conditioning	JEDEC Level 2 @ 260°C	3X
HAST	130°C / 85% RH	96 Hrs
Temp Cycle	Condition B -55 °C/125 °C	1000 cycles
High Temp Storage	150°C	1000 hours
Temp. Humidity Stress	85°C / 85% RH	1000 hours

The QFN Cu leadframe has 0.5 micro-inch Palladium plating (µ-PPF) layer and is Pb-free. The µ-PPF eliminates the solder-plating process and it enables to produce Pb-free product with the characteristics of superior bondability, solderability and crack-free forming. The package can withstand 3X reflow at 260degC.

The general PCB design rules for lead-free solder and Sn/Pb solder applications are the same rules. Only the board surface finish and the board material have to be considered for lead-free application due to the higher reflow temperature and lead-free solder compatibility. The PCB footprint design does not need to change for Pb-free assembly.

In order to perform at peak, special considerations are needed to properly design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, the exposed pad on the package needs to be soldered to the board using a corresponding thermal pad on the board. Furthermore, for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region. The PCB footprint design needs to be considered from dimensional tolerances due to package, PCB, and assembly.

A number of factors may have a significant effect on mounting QFN package on the board and the quality of solder joints. Some of these factors include: amount of solder paste coverage in exposed ground/thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow profile. This applications note provides the guidelines for this purpose. It should be emphasized that this is just a guideline to help the user in developing the proper motherboard design and surface mount process. Actual studies as well as development effort maybe needed to optimize the process as per user's surface mount practices and requirements.

4 External Interfaces

NMI120 uses an external 2 pin I2C interface described below:

4.1 I²C Interface

4.1.1 Overview

NMI120 provides an I²C bus slave that allows the host processor to read or write any register in the chip. NMI120 supports I²C bus Version 2.1 – 2000.

The I²C interface, used primarily for control, is a two-wire serial interface consisting of a serial data line (SDA, Pin 36) and a serial clock (SCL, Pin 35). It responds to the seven bit address values described in Section 4.1.3. The NMI120 I²C interface can operate in standard mode (with data rates up to 100 Kb/s) and fast mode (with data rates up to 400 Kb/s).

The I²C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data is transmitted in byte packages.

For specific information, please refer to the Philips Specification entitled “The I²C -Bus Specification, Version 2.1”.

4.1.2 I²C Timing

The I²C timing is provided in Figure 6 and Table 10.

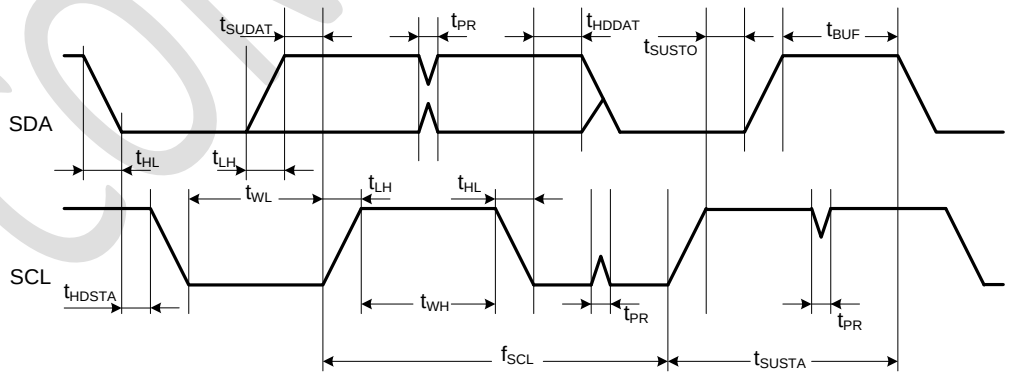

Figure 6: NMI120 I²C Timing Diagram

Table 10: NMI120 I²C Timing Parameters

Parameter	Symbol	Min	Max	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6		µs	
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300	ns	This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6		µs	
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0	900	ns	
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3		µs	
Glitch Pulse Reject	t_{PR}	0	50	ns	

4.1.3 I²C Slave Address

The NMI120 default I2C slave address is 0x67. This can be modified at customer's request.

5 Device States

5.1 Power Up/Down Requirements

The NMI120 has simple power up requirements regulated by the CHIP_EN pin. Following the guidelines below will ensure the proper start up and functioning of the NMI120.

5.1.1 Power Up

In the NMI120, the power supplies can be brought up in any order. There are, however, requirements that must be considered at power up. Please refer to Table 11.

- Each supply must obey the power up rise requirement of 10 ms (see Table 11).
- The CHIP_EN signals must remain at logic zero until all power supplies are stable. The timing of CHIP_EN starts after the last power supply has been brought to within specifications.
- The I2C can start to communicate with the tuner after a period of time (t_{CEI2C}) from which the CHIP_EN is asserted. This time is used to provide an internal reset to the chip.

These requirements are summarized in Figure 7 and Table 11.

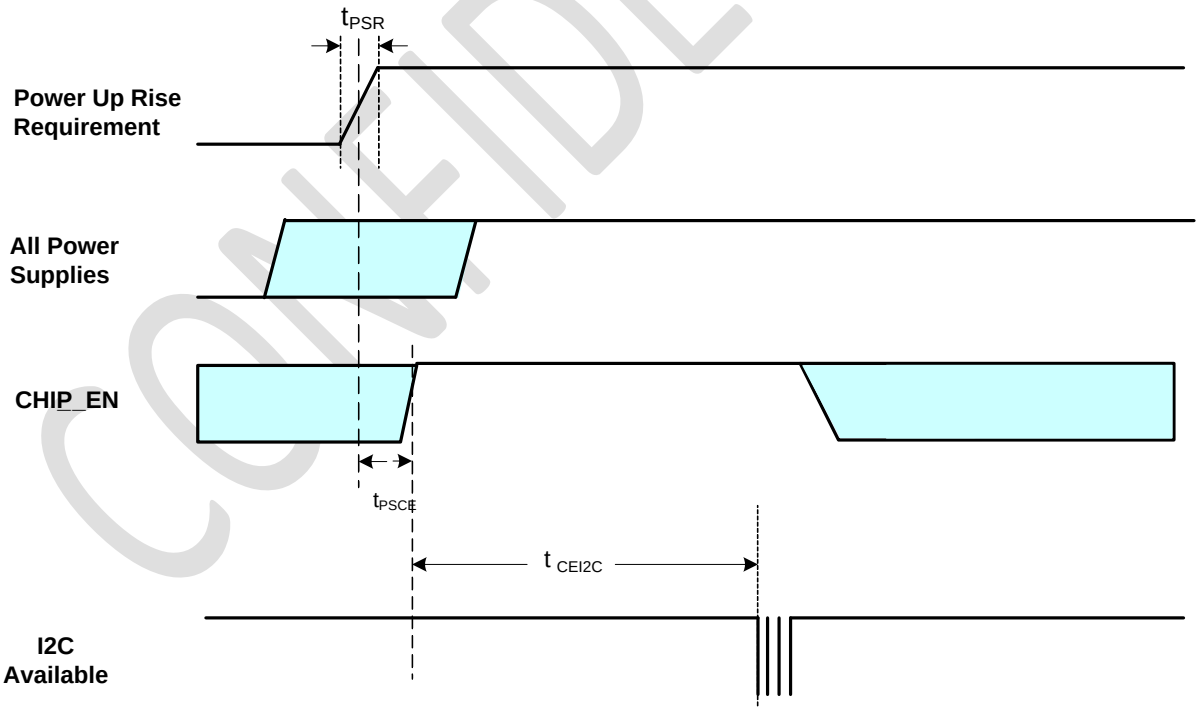

Figure 7: NMI120 Power-Up Sequence

Table 11: NMI120 Power-up Sequence Timing

Parameter	*Min*	*Max*	*Units*	*Description*	*Notes*
t_{PSR}		10	ms	Power Supply rise	t_{PSR} is measured from 10% to 90%
t_{PSCE}	50		ms	Power Supply stable to Chip Enable asserted	All power supplies must be stable before measuring timing
t_{CEI2C}		100	ms	Chip Enable to I2C communication.	

5.1.2 Power Down

There are no restrictions for power down.

6 Application Schematic

Please contact your NMI representative