SONY

TV Tuner IC

CXD2861ER

Description

The CXD2861ER is a silicon tuner which includes all the necessary functions such as RF amplifier, channel separation filter and other functions to receive terrestrial and cable TV broadcast programs.
The CXD2861ER provides low noise, low spurious, excellent protection ratio to interference and high reception sensitivity.
By integrating LNA / Balun function into the IC, the CXD2861ER lowers BOM cost and achieves the easy on-board integration.

Applications

- Analogue and digital TV tuner
- Analogue and digital tuner for PVR or STB

Features

- 75 Ω single-end input
- Low Phase Noise PLL synthesizer (DVB-C2 ready)
- Low distortion RF AGC amplifier
- High image interference rejecting function
- Channel selectable filter equivalent to SAW filter
- High output dynamic range IFAGC amplifier
- Wide band RF AGC circuit
- RF level measurement function
- 2.5~3.3 V flexible single power supply operation
- Small package (32 pin VQFN 5x5 mm)
- Two selectable IF output port
- Simple command interface for easy operation

Structure

CMOS silicon monolithic IC

Note) This IC has pins whose electrostatic discharge strength is weak as the high-frequency process is used.
Handle the IC with care.

E12830

Contents

1. Block Diagram ---- 3
2. Pin Description ---- 4
3. Electrical Characteristics Measurement circuit ---- 11
4. Application Circuit ---- 12
5. Absolute Maximum Rating ---- 13
6. Operating condition ---- 13
7. Electrical Characteristics ---- 14
7-1. General (Conditions) ---- 14
7-2. Electrical Characteristics 1 ---- 15
7-3. Electrical Characteristics 2 ---- 16
7-4. Electrical Characteristics 3 ---- 18
7-5. Electrical Characteristics 4 ---- 19
8. Circuit Block diagram ---- 20
8-1. AGC ---- 20
8-1-1. AGC Block diagram ---- 20
8-2. PLL ---- 21
8-2-1. Channel selection method ---- 21
8-3. RFVGA ---- 22
8-3-1. RFVGA Block diagram, ---- 22
8-3-2. Gain Control Range ---- 22
8-3-3. RFVGA Reception Frequency ---- 22
8-4. Channel Select Filter ---- 23
8-4-1. Channel Select Filter Register Setting ---- 24
8-5. IFVGA ---- 25
8-5-1. IFVGA Gain Control Range ---- 25
8-6. I^2C register composition ---- 26
9. Typical performance example ---- 27
10. Package Outline ---- 28
11. Mark ---- 29

1. Block Diagram

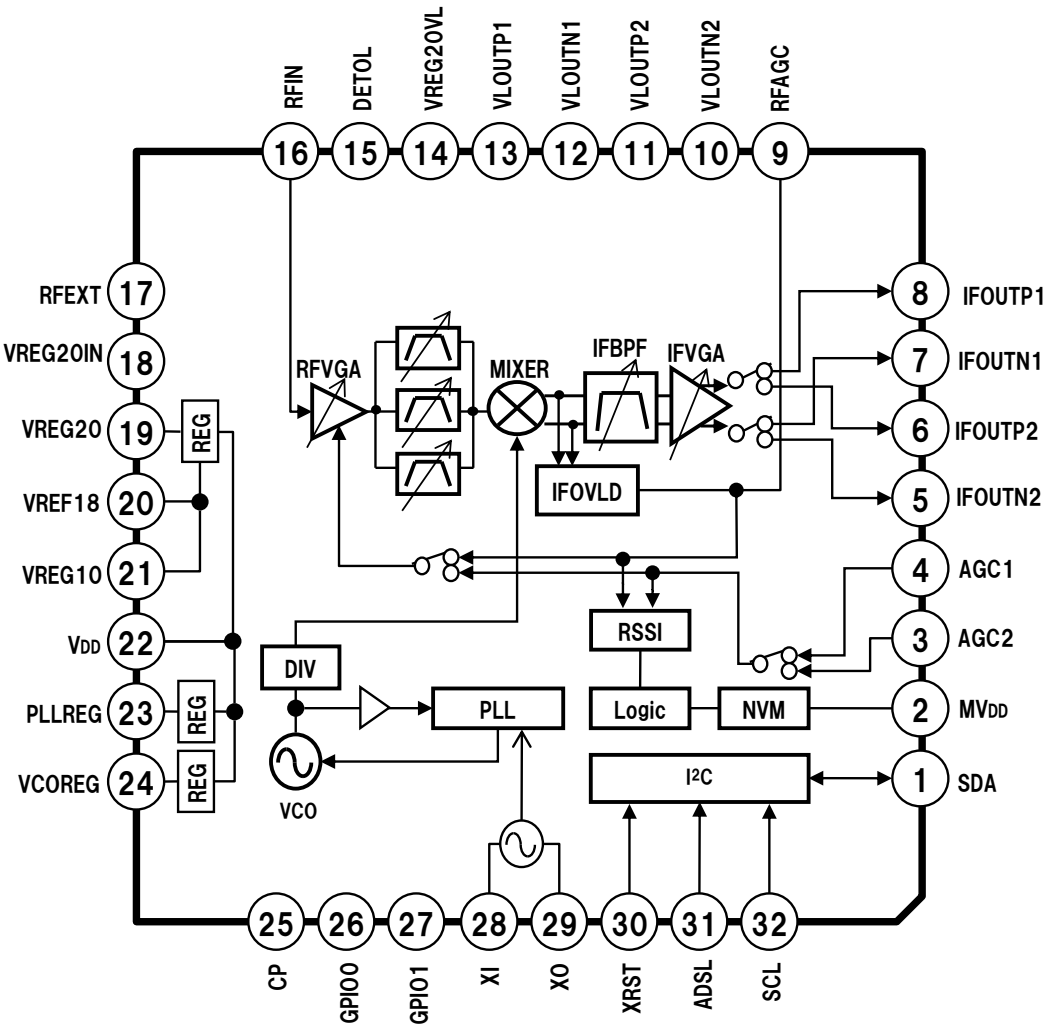
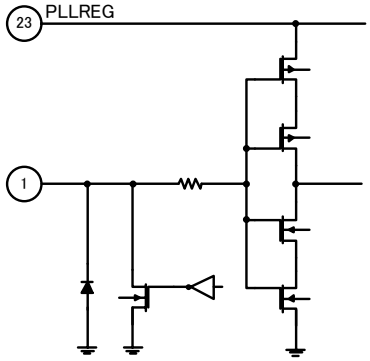
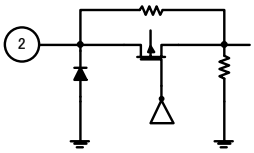
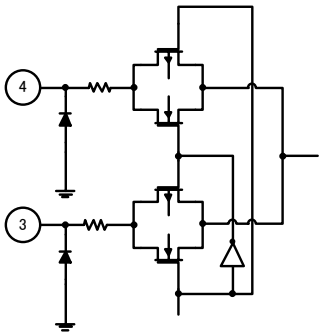
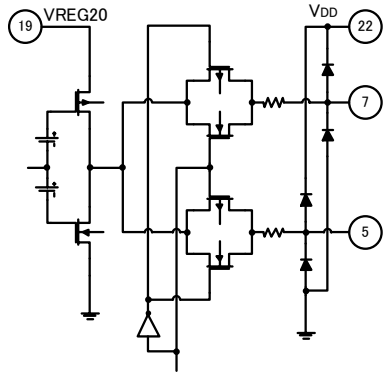
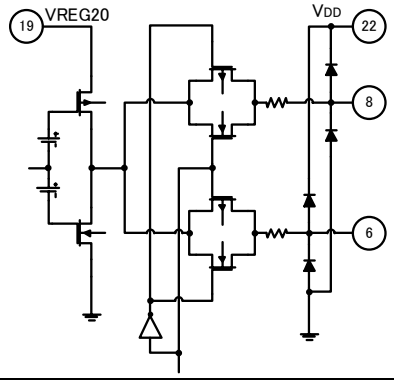
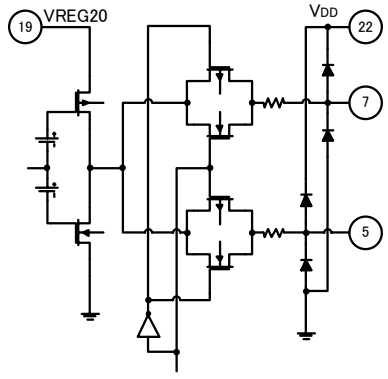
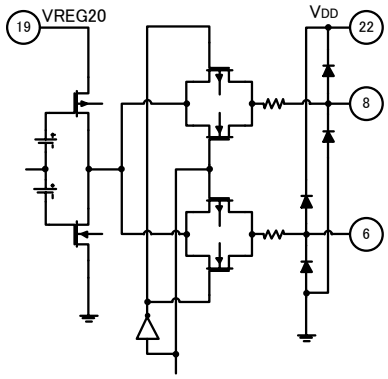
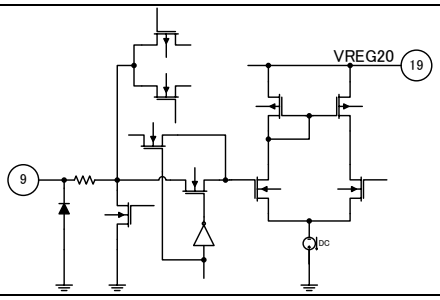
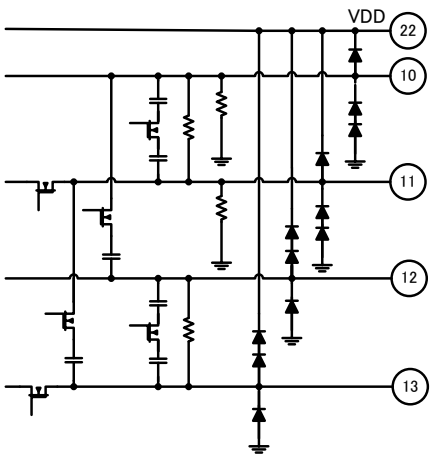


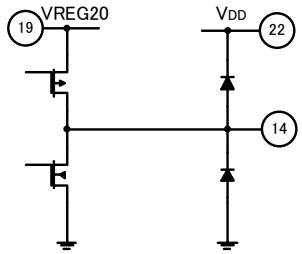
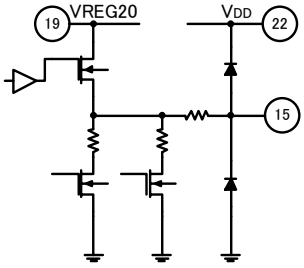
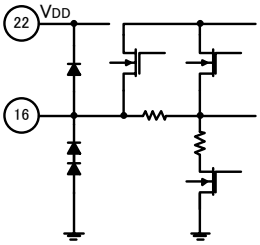
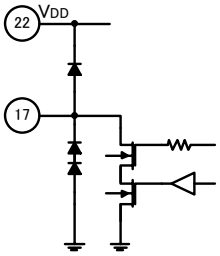
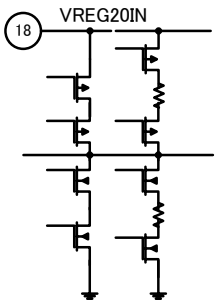
Fig.1. Block Diagram of CXD2816ER

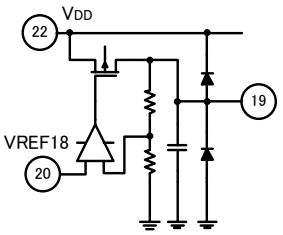
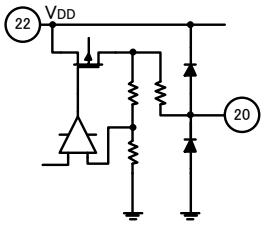
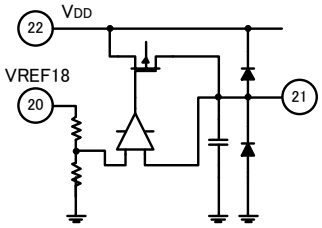
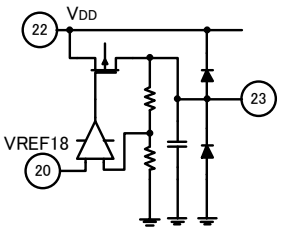
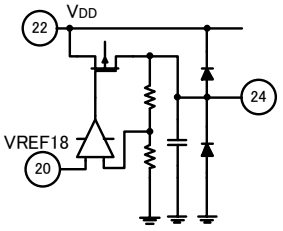
2. Pin Description

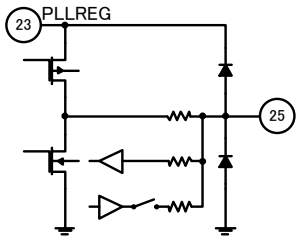
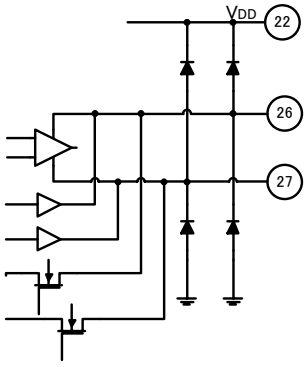
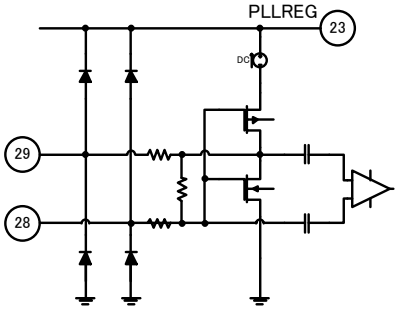
Pin No	Symbol	Pin Voltage [V]	Equivalent circuit	Description
1	SDA	Hi-Z		I^2C bus DATA input
2	MV_{DD}	0.0		Test port
3	AGC2	0.0~1.8		IFVGA and RFVGA gain control. Select 3-pin or 4-pin by register setting
4	AGC1	0.0~1.8		

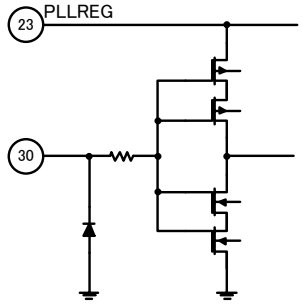
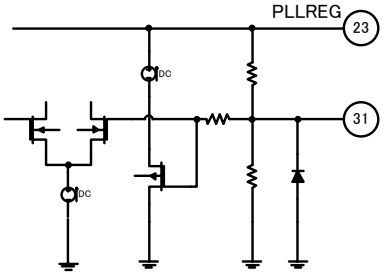
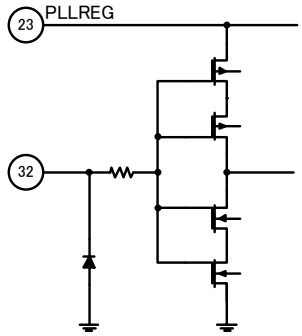
Pin No	Symbol	Pin Voltage [V]	Equivalent circuit	Description
5	IFOUTN2	1.0		IF output terminal. Either Pin-5 / Pin-6 or Pin-7 / Pin-8 differential output could be chosen by the setting of the register
6	IFOUTP2	1.0		IF output terminal. Either Pin-5 / Pin-6 or Pin-7 / Pin-8 differential output could be chosen by the setting of the register
7	IFOUTN1	1.0		IF output terminal. Either Pin-5 / Pin-6 or Pin-7 / Pin-8 differential output could be chosen by the setting of the register
8	IFOUTP1	1.0		IF output terminal. Either Pin-5 / Pin-6 or Pin-7 / Pin-8 differential output could be chosen by the setting of the register

Pin No	Symbol	Pin Voltage [V]	Equivalent circuit	Description
9	RFAGC	0.0~2.0		Terminal to connect ripple rejection capacitor for internal RFAGC feed back loop
10	VLOUTN2	0.0		Terminal for Secondary Inductor for Tracking filter at the output of the RFVGA of the VHF Low band.
11	VLOUTP2	0.0		Terminal for Secondary Inductor for Tracking filter at the output of the RFVGA of the VHF Low band
12	VLOUTN1	0.0		Terminal for Primary Inductor for Tracking filter at the output of the RFVGA of the VHF Low band
13	VLOUTP1	0.0		Terminal for Primary Inductor for Tracking filter at the output of the RFVGA of the VHF Low band

Pin No	Symbol	Pin Voltage [V]	Equivalent circuit	Description
14	VREG20VL	0.0 / 2.0		Regulated power supply terminal of RFVGA of the VHF Low band
15	DETOL	0.0~2.0		Terminal to connect ripple rejection capacitor for internal l RFAGC feed back loop
16	RFIN	0.0		Terminal for RF input
17	RFEXT	0.0		Terminal for external circuit control
18	VREG20IN	2.0		Regulated power supply for RFVGA

Pin No	Symbol	Pin Voltage [V]	Equivalent circuit	Description
19	VREG20	2.0		Terminal for voltage regulator used for analogue functional blocks
20	VREF18	1.8		Terminal for voltage regulator. Put decoupling capacitor to this Pin
21	VREG10	1.0		Terminal for voltage regulator used for analogue functional blocks
22	VDD	2.5		Power supply terminal
23	PLLREG	1.9		Terminal for voltage regulator used for PLL and Logic
24	VCOREG	1.8		Terminal for voltage regulator used for VCO

Pin No	Symbol	Pin Voltage [V]	Equivalent circuit	Description
25	CP	0.0~1.8		Charge pump output terminal External loop filter would be connect to this terminal
26	GPIO0	0.0~-1.9		General purpose output
27	GPIO1	0.0~1.9		
28	XI	0.9		Terminals for crystal connection of the reference oscillator
29	XO	0.9		

Pin No	Symbol	Pin Voltage [V]	Equivalent circuit	Description
30	XRST	Hi-Z		Hardware reset terminal (Negative Logic)
31	ADSL	1.45		Terminal for slave address selection of the I^2C BUS
32	SCL	Hi-Z		I^2C bus CLOCK input

3. Electrical Characteristics Measurement circuit

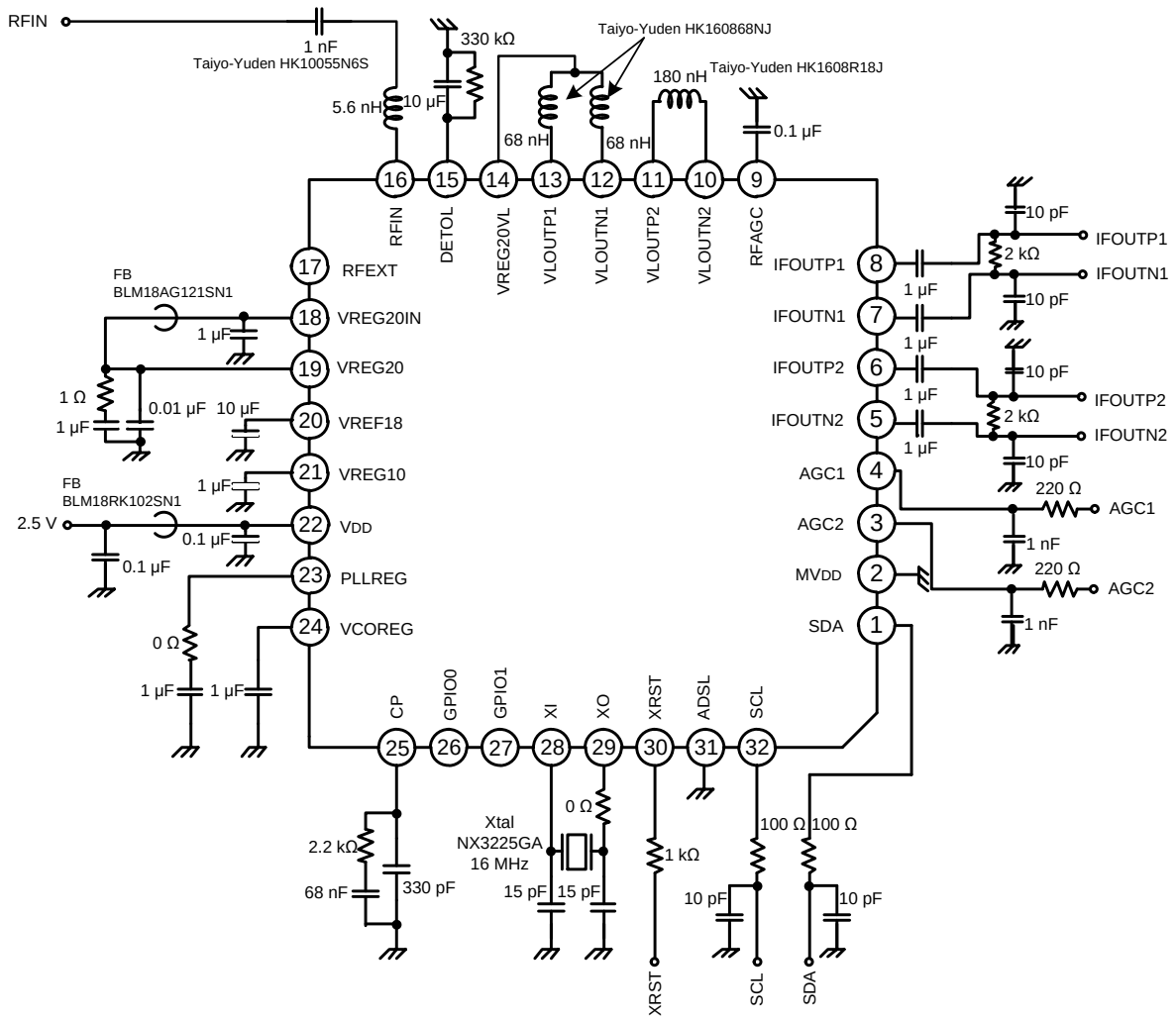


Fig.2. Electrical Characteristics Measurement Circuit

4. Application Circuit

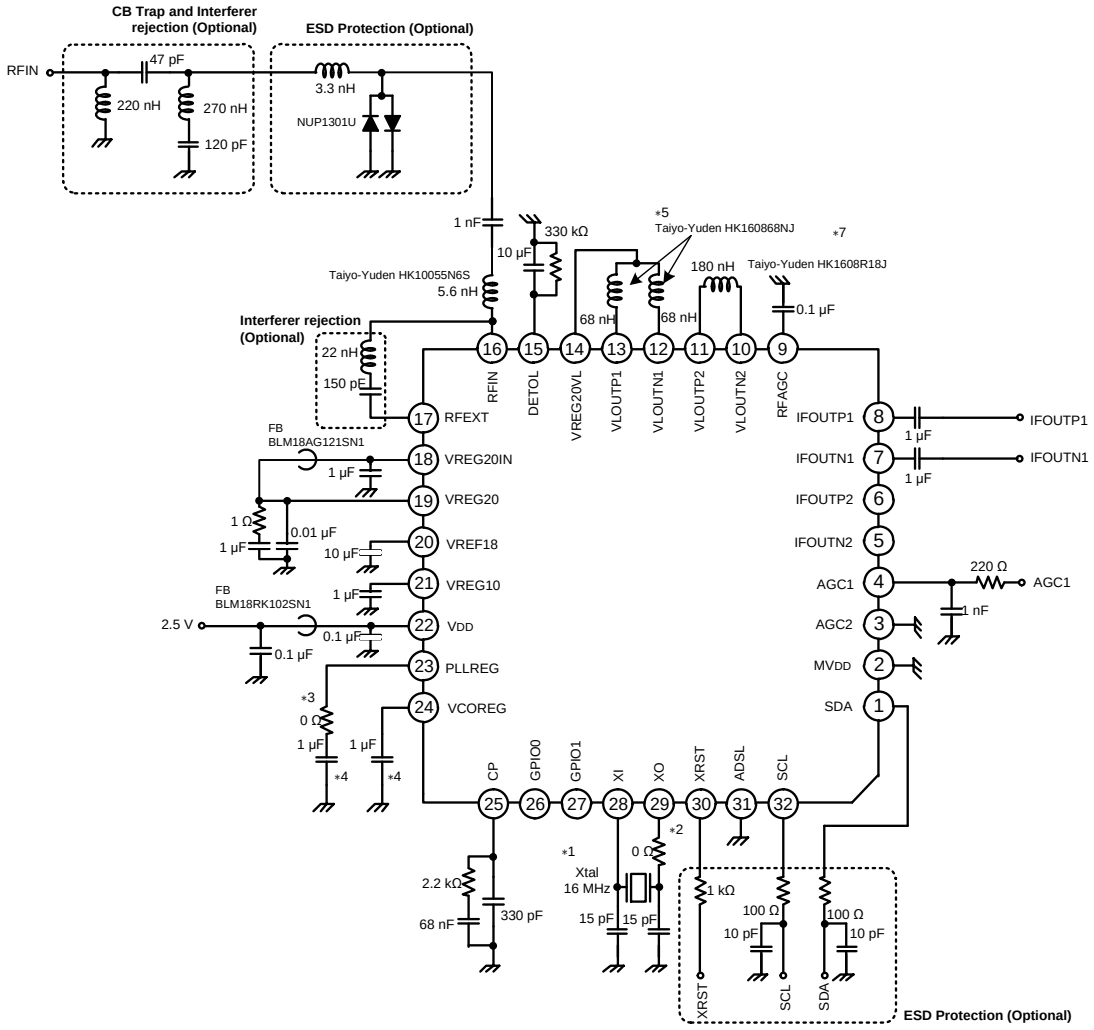


Fig.3. Electrical Characteristics Measurement Circuit

*1 AT-41 or NX3225GA is recommended for the crystal.

*2 Recommended to reserve lands for a resistor to suppress higher-order overtone oscillation.

*3 To suppress clock spurious, the series dumping resistor to PLLREG, can be useful.

The resistor value of ≦ 2.2 Ω is recommended.

*4 Put decoupling capacitors near the IC.

*5 Separate each inductors more than the parts dimension.

*6 The filter optimum values depend on the supported RF frequency and interferer suppression.

*7 The RF performances depend on the board layout. Refer to the hardware application note for actual board designing.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

5. Absolute Maximum Rating

Item	Symbol	Min.	Max.	unit
Supply Voltage	V_{DD}_ABS	-0.3	+3.6	V
AGC1/AGC2(AGC) Input Voltage	VAGC	-0.3	+3.6	V
SDA/SCL(I^2C) Input Voltage	VI2C	-0.3	+3.6	V
XRST Input Voltage	VXRST	-0.3	+3.6	V
RF input level	PM_ABS	-	+10	dBm

Absolute Maximum Input voltage for all the PINs apart from the PINs specified in the table above is -0.3 to +2.4 V

6. Operating condition

Item	Symbol	Min.	Max.	unit
Storage Temperature	Tstg	-55	+125	℃
Operation Temperature	Topr	-25	75	℃
Power Dissipation *1	PD	-	2.5	W

*1 Value when the device soldered onto the 30 mm × 60 mm, t = 1.0 mm, 4 Layer board

7. Electrical Characteristics

7-1. General (Conditions)

Item	Conditions
Reception frequency range	42 ~ 1002 MHz
Power supply voltage(VDD)	2.5 +/- 0.125 V or 3.3 +/- 0.3V
RF input level	-88 ~ +5 dBm
IF center frequency	3.55 ~ 5.5 MHz
IF frequency band width	5.65 ~ 8.8 MHz
IF output level	0.23 Vrms (differential output level)*2
IF maximum output level	4.0 Vp-p (differential output level) *2
AGC voltage range	0 ~ 1.8 V
Crystal frequency	16 MHz / 24 MHz *1
External reference frequency	16 MHz / 24 MHz / 41 MHz *1
Input level in external reference application	0.35 Vp-p < VXI ≦ 1.5 Vp-p *3
Maximum jitter in external reference application	< 10 ps
Input capacitor value of XI terminal in external reference application	< 5 pF
Data interface	I^2C Bus interface

*1 Recommend verification of the matching of the crystal application circuit communicating with crystal vendor.

*2 Under the condition of 1 kΩ // 10 pF single ended load is added at the IFOUT to the GND.

*3 Level at Pin28 (XI) when Pin29 (XO) is AC grounded.

7-2. Electrical Characteristics 1

(Circuit voltage = 2.5 V, Ta = 25 ˚C) (See the Electrical Characteristics Measurement Circuit)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
IFOUT pin						
IFOUT output voltage	VcmIF		0.95	1.0	1.05	V
DETOL pin						
High level output voltage	VDETOLH	Internal RFAGC is activated (OverLoad)	0.6 *1		2.0 *1	V
Low level output voltage	VDETOLL	For no RF signal input	GND		0.2	V
SDA, SCL and XRST pins						
High input voltage	VIH		2.3		3.6	V
Low input voltage	VIL		-0.3		1	V
Terminal leak current		Terminal voltage = 3.6 V			10	µA
SDA pin						
Low output voltage	VOL1	Sink current : 3 mA	GND		0.4	V
GPIO pin						
High output voltage	GPH	Source current : 3 mA	1.7	1.9		V
Low output voltage	GPL	Sink current : 3 mA		0.0	0.2	V
Drive current	Idrive	Source current / Sink current			3	mA
AGC pin						
Terminal leak current	IsAGC	Sink current at AGC voltage = 3.6 V			200	µA

*1 Output voltage of the DETOL terminal varies by the level of the interferer.

Refer to the separated Application Note for details.

7-3. Electrical Characteristics 2

(Circuit voltage = 2.5 V, Ta = 25 ˚C, In case of no instructions, apply System-B/G Analog mode setting)

(See the Electrical Characteristics Measurement Circuit)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current 1 during normal operation	IDD1	VDD current, AGC voltage = 0.6 V, RF = 866 MHz	183	245	307	mA
Circuit current 2 during standby mode	IDD2	VDD standby mode current, AGC voltage = 0.6 V		12	21	mA
Conversion gain 1 *1 *2	GC1	RF = 50.5 MHz, IF = 5.05 MHz, AGC voltage = 0 V	79	82	85	dB
Conversion gain 2 *1 *2	GC2	RF = 449 MHz, IF = 5.05 MHz, AGC voltage = 0 V	82	85	88	dB
Conversion gain 3 *1 *2	GC3	RF = 866 MHz, IF = 5.05 MHz, AGC voltage = 0 V	80	83	86	dB
Conversion gain 4 *1 *2	GC4	RF = 1002 MHz, IF = 5.05 MHz, AGC voltage = 0 V		78		dB
In-band filter level deviation VL1 *4	RFwvl1	RF = 50 MHz, VHF-L	-1.5	-1	0.5	dB
In-band filter level deviation VL2 *4	RFwvl2	RF = 93 MHz, VHF-L	-1.5	-1	0.5	dB
In-band filter level deviation VL3 *4	RFwvl3	RF = 192 MHz, VHF-L	-1.5	-1	0.5	dB
In-band filter level deviation VH1 *4	RFwvh1	RF = 192.1 MHz, VHF-H	-1.5	0	0.5	dB
In-band filter level deviation VH2 *4	RFwvh2	RF = 504 MHz, VHF-H	-1.5	0	0.5	dB
In-band filter level deviation U1 *4	RFwu1	RF = 504.1 MHz, UHF	-1.5	0	0.5	dB
In-band filter level deviation U2 *4	RFwu2	RF = 866 MHz, UHF	-1.5	0	0.5	dB
Noise figure 1-1 *2	NF1-1	RF = 50.5 MHz, IF = 5.05 MHz, AGC voltage = 0 V		5.2	6.0	dB
Noise figure 1-2 *2	NF1-2	RF = 449 MHz, IF = 5.05 MHz, AGC voltage = 0 V		4.1	6.0	dB
Noise figure 1-3 *2	NF1-3	RF = 866 MHz, IF = 5.05 MHz, AGC voltage = 0 V		4.7	6.0	dB
Noise figure 1-4 *2	NF1-4	RF = 1002 MHz, IF = 5.05 MHz, AGC voltage = 0 V		5.5		dB
Noise figure 2-1 *2	NF2-1	RF = 50.5 MHz, IF = 5.05 MHz, DVB-T Digital mode *3, AGC voltage = 0 V		4.8	5.5	dB
Noise figure 2-2 *2	NF2-2	RF = 449 MHz, IF = 5.05 MHz, DVB-T Digital mode *3, AGC voltage = 0 V		4.0	5.0	dB
Noise figure 2-3 *2	NF2-3	RF = 866 MHz, IF = 5.05 MHz, DVB-T Digital mode *3, AGC voltage = 0 V		4.4	5.0	dB
Noise figure 2-4 *2	NF2-4	RF = 1002 MHz, IF = 5.05 MHz, DVB-T Digital mode *3, AGC voltage = 0 V		5.2		dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Return loss	RL	RF = 866 MHz AGC voltage = 0.6 V		10	8	dB
CTB	CTB	RF = 866 MHz RF level = -34 dBm 134tone		-65		dBc
CSO	CSO	RF = 866 MHz RF level = -34 dBm 134tone		-65		dBc
RFAGC range *2	RFAGC	RF = 866 MHz AGC voltage = 0.6~1.8 V	68	72		dB
IFAGC range *2	IFAGC	AGC voltage = 0.0~0.6 V	27	30		dB
AGC range *2	AGC	RF = 866 MHz AGC voltage = 0.0~1.8 V	95	102		dB
AGC control sensitivity *2	AGCS	RF = 866 MHz AGC voltage = 0.1~1.3 V	-250	-70	-5	dB/V
Image rejection ratio *2	IMRR	RF = 866 MHz IF = 5.05 MHz		-70	-60	dBc
PS beat 3rd order *2	PS3	AGC voltage = 0.9 V		-75	-65	dBc
PS beat 2nd order *2	PS2	AGC voltage = 0.9 V		-75	-65	dBc
IF filter attenuation *2	IFATT	Level attenuation at IF = 7.15 MHz relative to IF = 4 MHz under IF band width = 6 MHz setting		-24	-22	dBc
IF in-band tilt 1 *2	IFTILT1	RF = 866 MHz Level difference at IF = 1.25 MHz relative to IF = 4 MHz	-1	0.5	2	dB
IF in-band tilt 2 *2	IFTILT2	RF = 866 MHz Level difference at IF = 5.75 MHz relative to IF = 4 MHz	2	-0.5	-1	dB

*1 CG = Read out from spectrum analyzer – display SG output.

*2 Under the condition of 1 kΩ//10 pF single ended load is added at the IFOUT to the GND.

*3 Refer to the annex application note for further explanation of the reception mode.

*4 Level deviation of the level at picture frequency (Fp = RF – 2.75 MHz) and level at croma frequency (Fc = Fp + 4.43 MHz).

7-4. Electrical Characteristics 3

(Circuit voltage = 2.5 V, Ta = 25 ˚C) (See the Electrical Characteristics Measurement Circuit)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Lock-in time	tLOCK	When locked RF = 1002 MHz			10	ms
STEP tuning range High *3	PSTEP_RANGE_H	RF for ≧ 90 MHz	-1.4		1.4	MHz
STEP tuning range Low *3	PSTEP_RANGE_L	RF for < 90 MHz	-0.4		0.4	MHz
Analog mode phase noise 1 *4	PNA1	10 kHz offset, RF = 866 MHz System-B/G Analog mode		-80	-75	dBc/Hz
Analog mode phase noise 2 *4	PNA2	100 kHz offset, RF = 866 MHz System-B/G Analog mode		-110	-105	dBc/Hz
Analog mode phase noise 1 *4	PND1	1 kHz offset, RF = 866 MHz DVB-T Digital mode		-92	-88	dBc/Hz
Analog mode phase noise 2 *4	PND2	10 kHz offset, RF = 866 MHz DVB-T Digital mode		-97	-93	dBc/Hz
Analog mode phase noise 3 *4	PND3	100 kHz offset, RF = 866 MHz DVB-T Digital mode		-105	-101	dBc/Hz

7-5. Electrical Characteristics 4

(Circuit voltage = 2.5 V, Ta = 25 ˚C) (See the Electrical Characteristics Measurement Circuit)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}		0		400	kHz
Start hold time	t_{HDSTA}		600			ns
Stop setup time	t_{SUSTO}		600			ns
Bus free time between "STOP" and "START" condition	t_{BUF}		1300			ns
Data setup time	t_{SUDAT}		100			ns
High hold time	t_{HIGH}		600			ns
Data hold time	t_{HDDAT}		0		900	ns
Low hold time	t_{LOW}		1300			ns
Start setup time	t_{SUSTA}		600			ns
Rise time	tr				300	ns
Fall time	tf				300	ns
Capacitive load of bus line	Cb				400	pF
Hard reset pulse width	t_{HR}	Input to 30pin(XRST)	1			ms

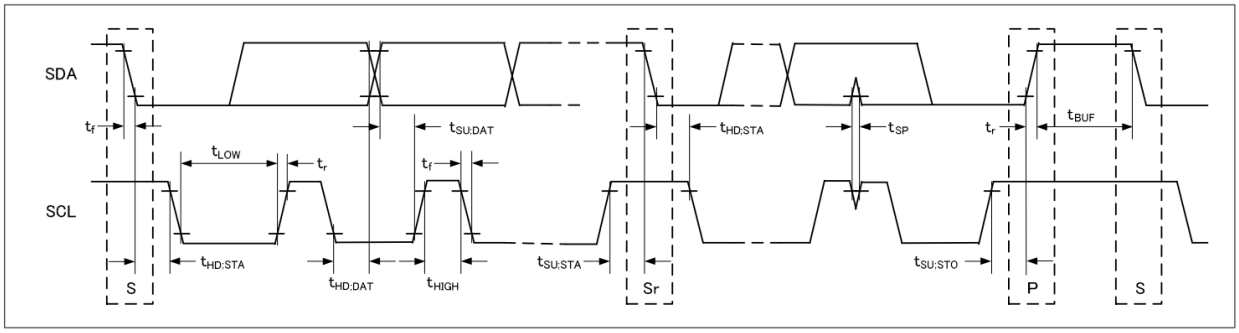


Fig.4. I^2C Interface

$t_{HD:STA}$ = Hold time(repeated) START condition

t_{Low} = LOW period of the SCL clock

$t_{HD:DAT}$ = Data hold time

$t_{SU:DAT}$ = Data setup time

t_{HIGH} = HIGH period of the SCL clock

$t_{SU:STA}$ = Setup time for a repeated START condition

t_{BUF} = Bus free time between a STOP and START condition

$t_{SU:STO}$ = Setup time for STOP condition

tr = Rise time of both SDA and SCL signals

tf = Fall time of both SDA and SCL signals

8. Circuit Block diagram

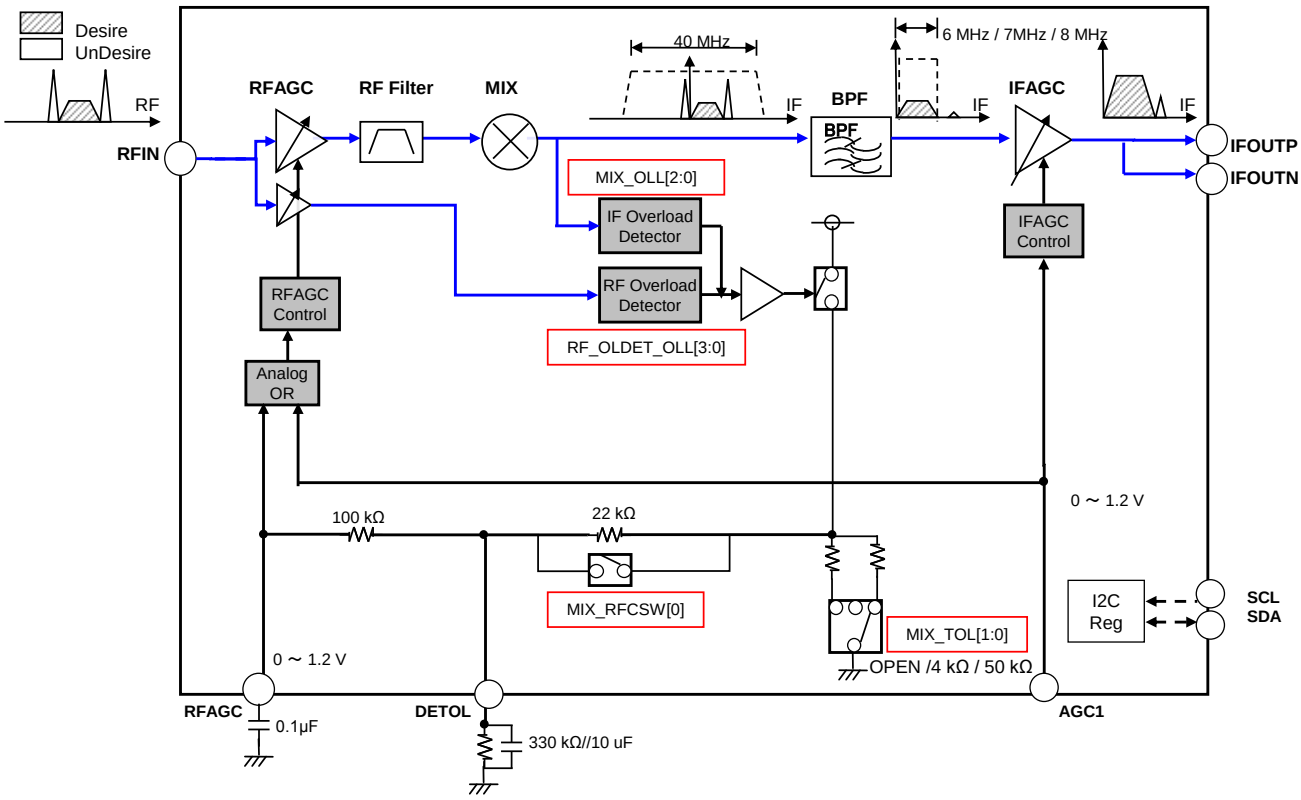
8-1. AGC

In the CXD2861ER, IF output level can be controlled to the specified level by applying appropriate AGC voltage. AGC system consists of cascaded RF VGA and IF VGA. As RF input power at the input of the RFin goes up, the gain of the IF VGA reduces the gain first then the gain of the RF VGA reduces second, in this manner the system maintains the high sensitivity and low distortion over the wide range of RF input level.

Also the CXD2861ER has level detector at the RF input and at the mixer out put. This detector can be applied to the internal RFAGC system as the detection signal.

Appropriate gain control is performed to prevent saturation of the circuit from out of band interference signal which can't be detected in IF output internally, and high protection performance is realized.

8-1-1. AGC Block diagram



Refer to the annex application note for further explanation of the registers

Fig.5. AGC block diagram

8-2. PLL

CXD2861ER implements Fractional-N PLL, and it preforms Low phase noise as well as precise frequency step size

8-2-1. Channel selection method

CXD2861ER automatically set the Local frequency by setting the RF reception frequency and the IF frequency in channel selection.

Local frequency and VCO frequency are function of the RF reception frequency and the IF frequency, and these are given by the equation below.

FLO=FRF+FIF

Symbol	Item	Min.	Typ.	Max.	Unit	Description
FRF	RF reception frequency	42		1002	MHz	Set the value in kHz step in FRF register
FIF	IF frequency	3.55		5.5	MHz	Select the bandwidth 6 MHz / 7 MHz / 8 MHz by setting the value in BW register Precise setting can be done in 50 KHz step size by setting the value in FIF_OFFSET register.
FLO	Local Frequency	45.7		1006	MHz	

Refer to the annex application note for further explanation of the registers

8-3. RFVGA

The CXD2861ER integrates RFVGA with low noise and low distortion characteristics and output tracking filters for each band.

8-3-1. RFVGA Block diagram,

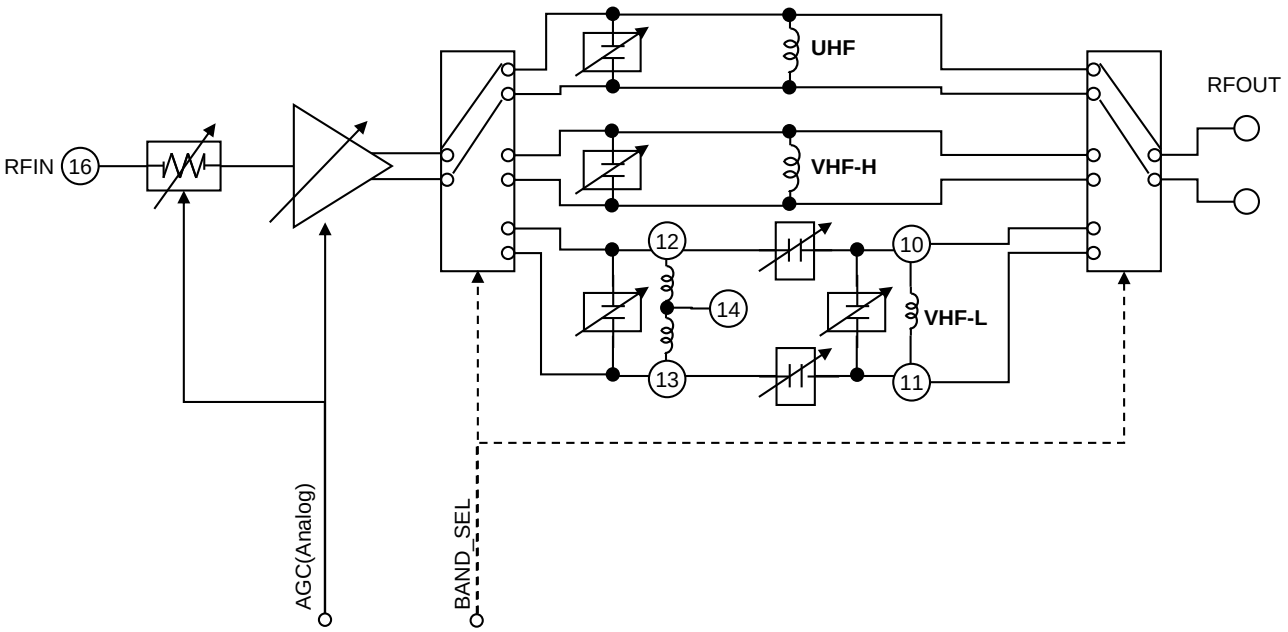


Fig.6. RFVGA Block diagram

8-3-2. Gain Control Range

Gain control range of the RFVGA is specified in the table below.

AGC (V)	Gain (dB)
0.6~1.4	21~-51 *1

*1 Center sample value.

8-3-3. RFVGA Reception Frequency

RF reception frequency range is divided into 3 bands.

Standard RF band classification

BAND_SEL	FRF（MHz）
UHF	504 ＜ FRF ≦ 1002
VHF-H	192 ＜ FRF ≦ 504
VHF-L	42 ＜ FRF ≦ 192

8-4. Channel Select Filter

The frequency response of the channel selection filter is illustrated in the figure below.

IF center frequency shall be changed when IF band width has changed due to the fixed lower cut off frequency of the band bass filter.

IF band width and IF center frequency can be adjusted individually by the setting of the register.

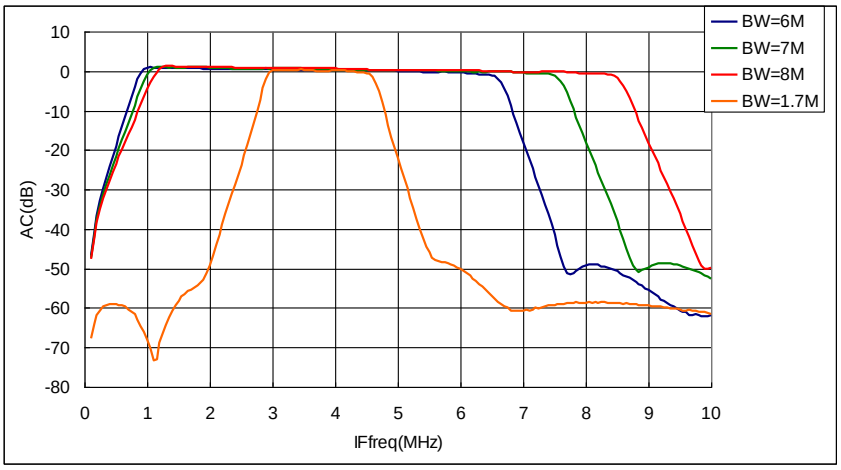


Fig.7. IF Frequency Response

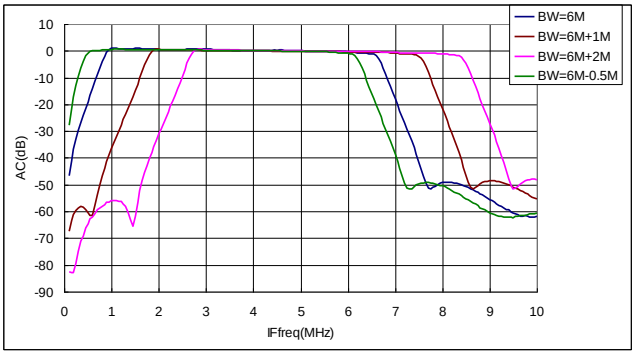


Fig.8. IF frequency Response (Filter offset 6M_mode)

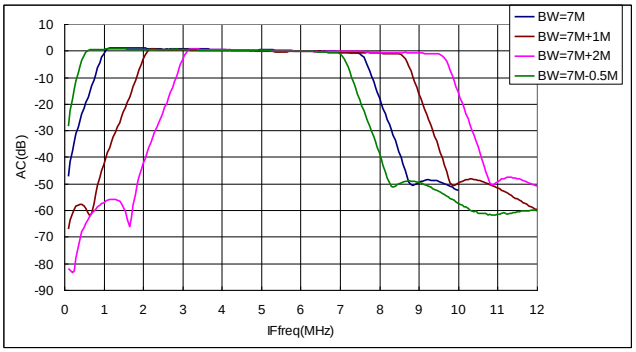


Fig.10. IF Frequency Response (Filter offset 7M_mode)

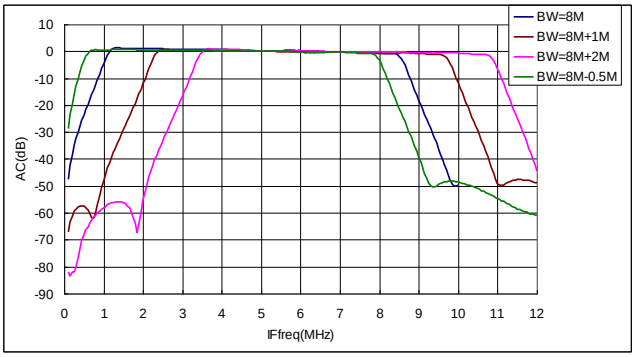


Fig.9. IF frequency Response (Filter off set 8M_mode)

8-4-1. Channel Select Filter Register Setting

Register Name	Note
BW	6M_mode : IF BandWidth = 6 MHz, IFc = 4.0 MHz （IFp = 5.75） 7M_mode : IF BandWidth = 7 MHz, IFc = 4.5 MHz （IFp = 6.75） 8M_mode : IF BandWidth = 8 MHz, IFc = 5.0 MHz （IFp = 7.75） 1.7M_mode ：IF BandWidth = 1.7 MHz, IFc = 3.7 MHz * IFc and IFp shows IF center frequency and IF picture carrier frequency respectively.
FIF_OFFSET	IF frequency offset adjustment value -750 kHz～+800 kHz /50 kHz step
BW_OFFSET	IF band width adjustment value 6M_mode/7M_mode/8M_mode：-750 kHz～+800 kHz /50 kHz step 1.7M_mode ：0 kHz fixed
IF_BPF_F0	IF center frequency offset setting Prohibit the setting in 1.7M_mode

Refer to the annex application note for further explanation of the registers

8-5. IFVGA

The CXD2861ER has two sets of IF output and AGC control pin to support multiple demodulators.

Either IFOUTP1, IFOUTN1 and AGC1 or IFOUTP2, IFOUTN2 and AGC2 could be active by the setting of the register.

Only one pair of IFOUTPUT and one AGC control can be chosen in the operation.

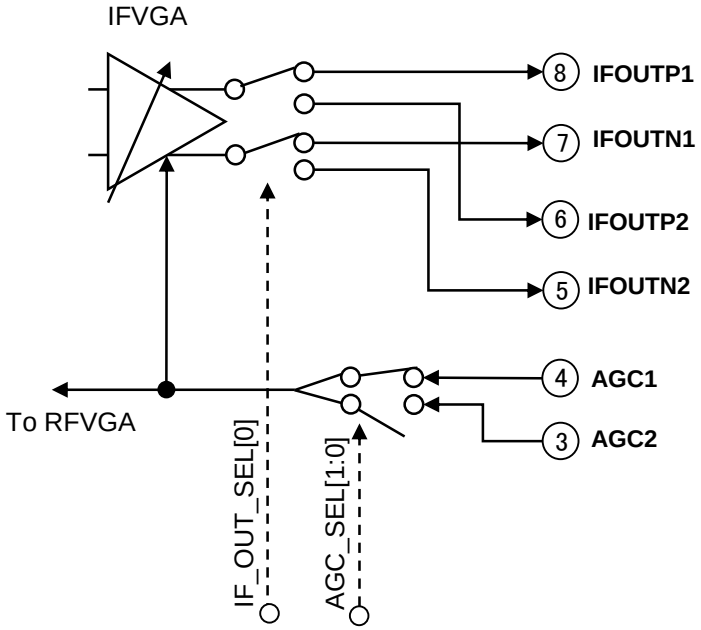


Fig.11. IFVGA Block diagram

Refer to the annex application note for further explanation of the registers

8-5-1. IFVGA Gain Control Range

Gain control range of the IFVGA is specified in the table below.

AGC (V)	Gain (dB)
0.0~0.6	36~6 *1

*1 Center sample value.

8-6. I²C register composition

The I²C bus interface is used to access from the host to CXD2861ER. CXD2861ER supports I2C bus Fast mode (400 kHz).

The slave address can be set by the voltage of Pin ADSL.

The voltage shall be produced by the resistance division between PLLREG ~ DGND.

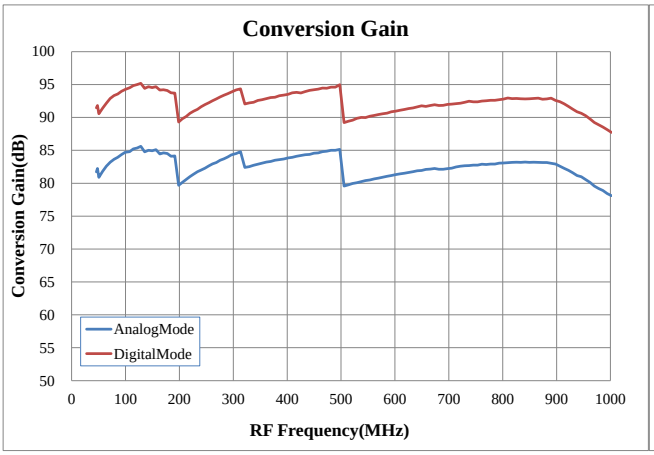
I²C Slave Address

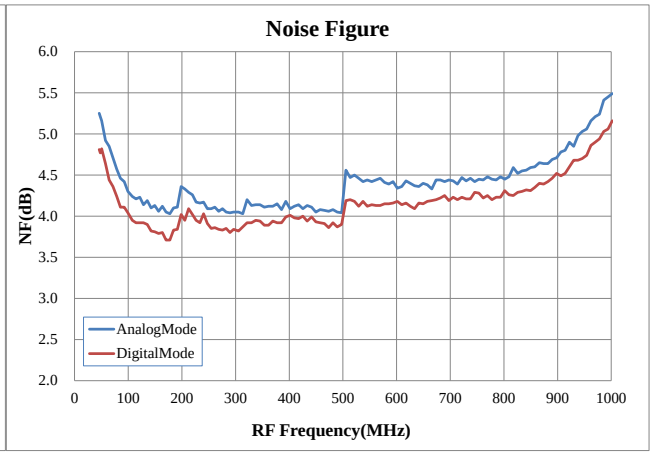
Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
1	1	0	0	0	MA1	MA0	R/W

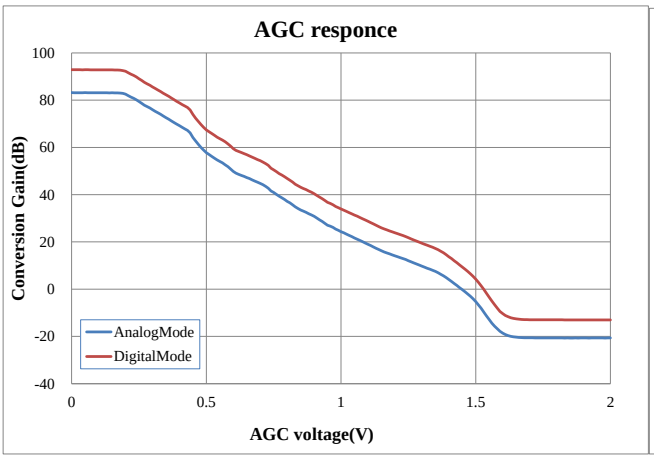
MA0/MA1 setting

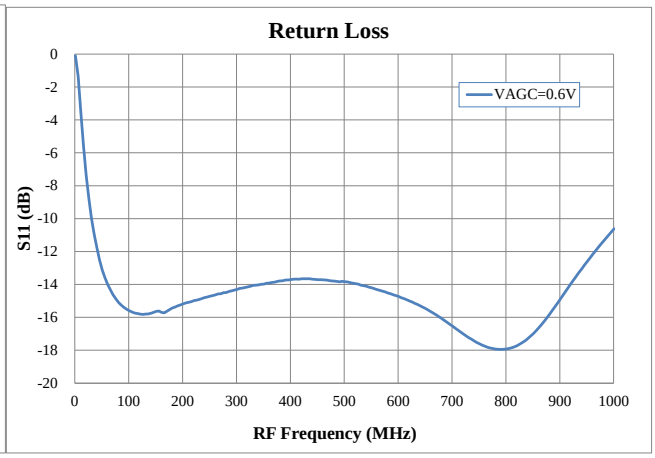
ADSL terminal voltage	MA1	MA0
0V ~ 0.19 V	0	0
Open	0	1
0.76V ~ 1.14 V	1	0
1.33V ~ 1.52 V	Do not use	
1.71V ~ 1.9 V	Do not use	

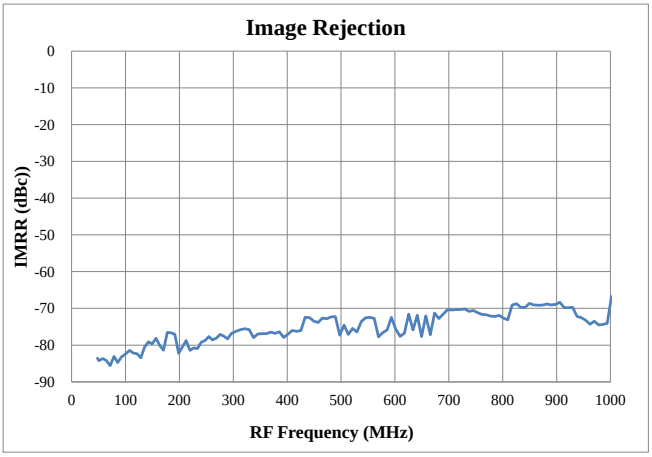
9. Typical performance example





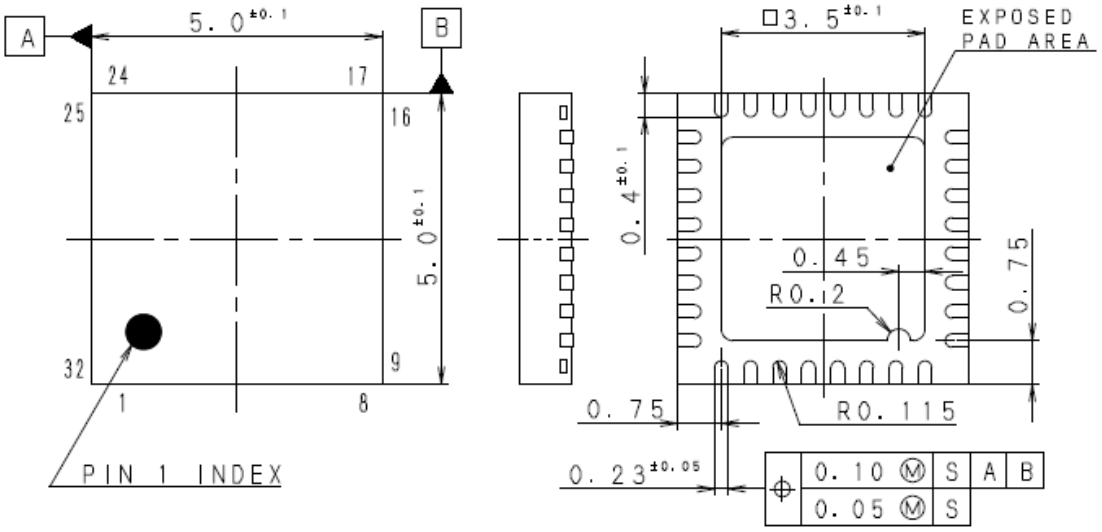


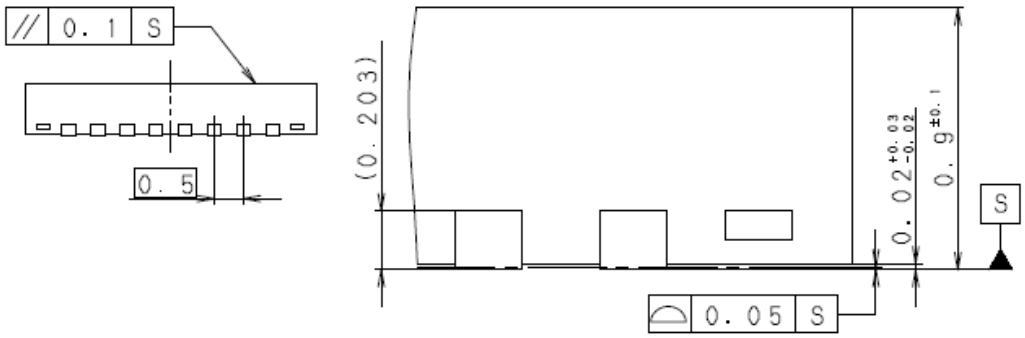




10. Package Outline

32PIN VQFN (PLASTIC)





TERMINAL SECTION

PACKAGE STRUCTURE

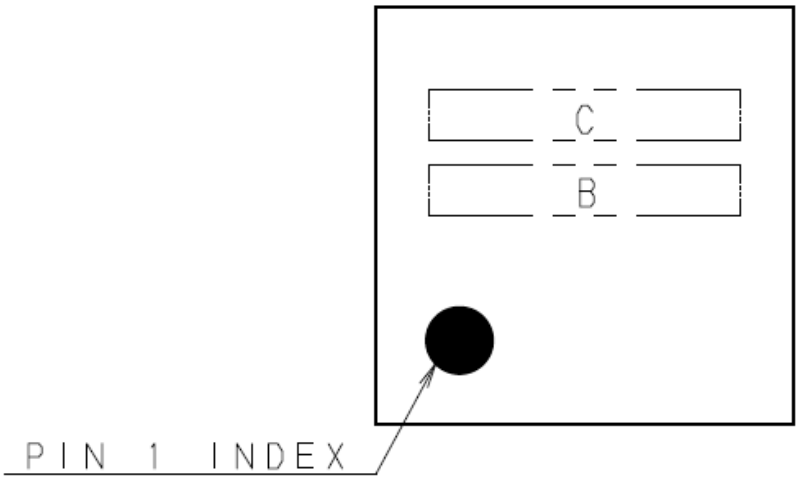
SONY CODE	VQFN-32P-401
JEITA CODE	P-VQFN32-5x5-0.5
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	Sn PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.071g

PART No. AP-2000-32QNAP1		Rev. 0
ISSUED '12.06.27	REVISED	
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.	
REMARKS PKG CODE:ER-32-PAP		

(Unit : mm)

11. Mark



MARKING C: D2861ER

注1） C部は製品名（Ｍａｘ７文字）を配置する。
（７文字を超える場合は製品名省略標示規定に従う。）
2） B部はロット番号（Ｍａｘ７文字）を配置する。

< INSTRUCTIONS >
1) TYPE NO. (MAX 7 CHARACTERS) IN SECTION C.
(FOR MORE THAN 7 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B.

IMPORTANT INFORMATION

Sony reserves the right to change products and specifications without prior notice.

Application circuits shown, if any, are typical examples illustrating the operation of the devices, they are shown for general guidance purposes and may not be specifically relevant to individual requirements. Therefore, whilst Sony endeavour to ensure that the information shown is as accurate as reasonably possible, Sony does not accept liability for any faults, damage or losses of any nature (including, but not limited, to consequential loss) arising from the use of the information contained in this document.

Customers considering the use of any device shown in this document in special applications where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, medical devices for life support, etc.) are recommended to consult with their Sony sales representatives before such use.